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Challenges of Atomic Force Probe Characterization of Logic Based Embedded DRAM for On-Processor Applications

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Abstract

Nanoprobing logic based SOI embedded DRAM cells for on-processor designs poses different challenges than probing conventional six transistor SRAM designs. This paper will describe nanoprobing logic based embedded DRAM (eDRAM) cells in 65nm SOI applications. We will also describe probe placement and measurement methodology for electrical characterization of leakage between deep trench capacitors composing those eDRAM designs. The introduction of nano CV metrology and scanning capacitance imaging for use in characterizing DRAM capacitors will also be discussed.

Introduction

The emergence of multiple core, high speed microprocessors in 90nm node technologies has also increased the requirement for large amounts of costly SRAM on-processor cache to avoid excessive finite cache penalties.

However, by employing Logic based on-processor embedded DRAM cache in 65nm SOI applications, limitations in SRAM cache involving standby current, requirements for error correction circuity to address soft error rate (SER), and Vmin cell stability can be overcome.[1-14] IBM has pioneered low cost embedded DRAM for SOI processors. [1,2]

Reported high performance embedded DRAM 65nm SOI designs with ~ 1.5ns latency and < 2ns random cycle characteristics are enabled by strain engineered pass transistor with optimized source/drain junctions for sub-pA off currents.[1-12]

Implementing a deep trench capacitor design versus a plate type design for embedded DRAM cache in these SOI designs means fewer mask steps (with lower cost) accompanied by a significantly smaller DRAM cell size.[1-2] Relative to SRAM, embedded DRAM cell size for 65nm SOI cache designs measures 0.127 μm^2 (vs. 0.299um^2 for SRAM) and for 45nm SOI cache measures 0.067 μm^2 (vs. 0.149um^2). These embedded DRAM cell sizes dramatically increase cache capacity (2Mb and 4Mb cache reported) while simultaneously reducing cost, power consumption, and soft error sensitivity as well as occupying a smaller size footprint.[1-2]

A common failure mechanism in embedded DRAM process is trench capacitor leakage. In particular, leakage between adjacent cells due to defects in the isolation is one example. Physical Failure Analysis (PFA) with microscopy after bit mapping is tricky as many defects are non-visual or 'Sub-Microscopic'. Even pA leakage levels will cause poor charge retention in eDRAM cells.

Nanoprobing can supplement and even replace PFA on such structures as long as the data is of sufficient integrity to place each failure in the correct category on a pareto chart. [16] Knowing what failure class to look for will also be key to correctly choosing which PFA technique to use for final root cause determination.

While the spacing between individual nodes within these DRAM cells is not as aggressive as six transistor SRAM cells for the same technology [25], nano probing said DRAM cells presents different measurement challenges.

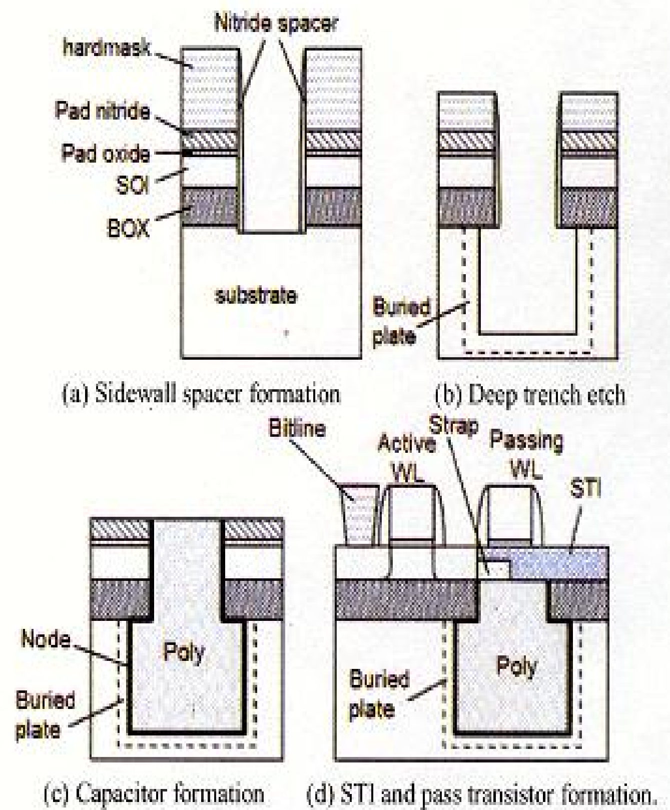

Figure 1
Novel Sidewall Spacer Deep Trench (SSDT) process.[1-5]

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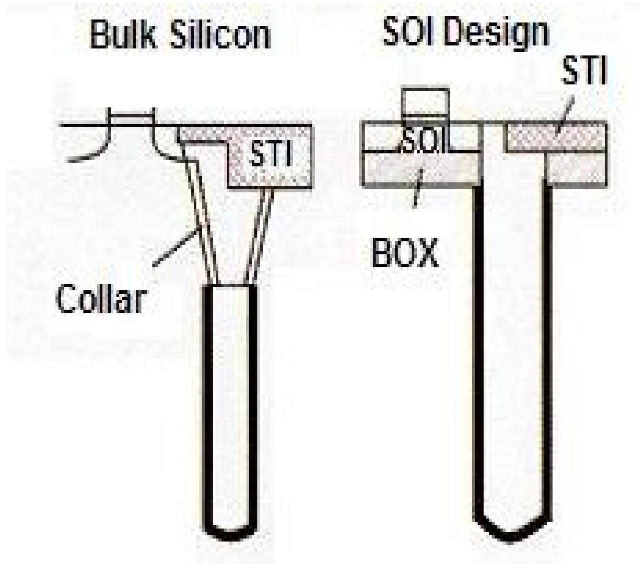

Figure 2
Comparison of Bulk Silicon eDRAM cell with SOI eDRAM cell (note elimination of collar in SOI design) [1, 2]

SOI eDRAM Description

Logic-based embedded DRAM cache on a high performance 65nm SOI platform involves a novel sidewall spacer deep trench (SDDT) process (Figure 1) that effectively provides low sheet and contact resistance. Low parasitic leakage is achieved by the superior SOI BOX isolation. The collar design used in bulk silicon deep trench is eliminated (Figure 2) resulting in a significantly lowered buried strap resistance.[1, 2] This IBM process is called Sidewall Spacer Deep Trench or SSDT.

Elimination of the collar from bulk silicon eDRAM trench design yielded significant reduction in strap resistance in the SOI design. A 15% Ion improvement is realized when the strap resistance is reduced from 3kΩ to 1kΩ [1, 2]

Employing a high performance SOI platform with deep trench capacitor design for Logic based embedded DRAM cache for on-processor applications has reduced cost, power consumption, while fitting in a smaller size footprint.[1,2]

Nanoprobing Challenges

The challenges to electrically characterize discrete embedded DRAM cells as small as 0.127μm^2 for 65nm SOI technologies and 0.067 μm^2 for 45nm SOI technologies requiring femto amp current sensitivities are not trivial.[16,17,18,19] In comparison, nanoprobing of six transistor SRAM cell arrays for 45nm SOI technologies may involve cell areas as small as 0.249 μm^2 however the larger cell size is filled with 6 transistors and 11 or 12 contacts resulting in an area with closer spacing between probes [25.] For DRAM, the challenges to nanoprobing are different; the bitlines are not in a regular pattern so that in order to insure the correct cell is probed:

1. the failed bitline must either be counted from a corner or mark,
2. a super high precision (50nm accuracy) stage must be used or,
3. a means of highlighting the leaking cell must be used for registration.

Counting is difficult and probing and marking of failed cells is not a good option for eDRAM because the mark is usually deposited in a FIB or SEM, potentially causing physical damage to the memory cell or electrical anomalies (eg. a short through the BOX layer in the case of SOI). It has become common practice to use AFM or AFP current imaging to localize defects.[17, 20] On SOI samples however, current imaging is not very effective since often (as in this paper) there is no current path to ground. Precision stage navigation works fine for locating previously bit mapped cell failures but it is severly limited in localizing unmapped defects. Therefore a cell to cell leakage analytical technique is highly preferred.

Deep Trench Capacitor Leakage Imaging with Two probe Current Imaging

In order to create an imaging technique capable of measuring trench to trench leakage, the imaging technique must highlight current passing between two bitlines.

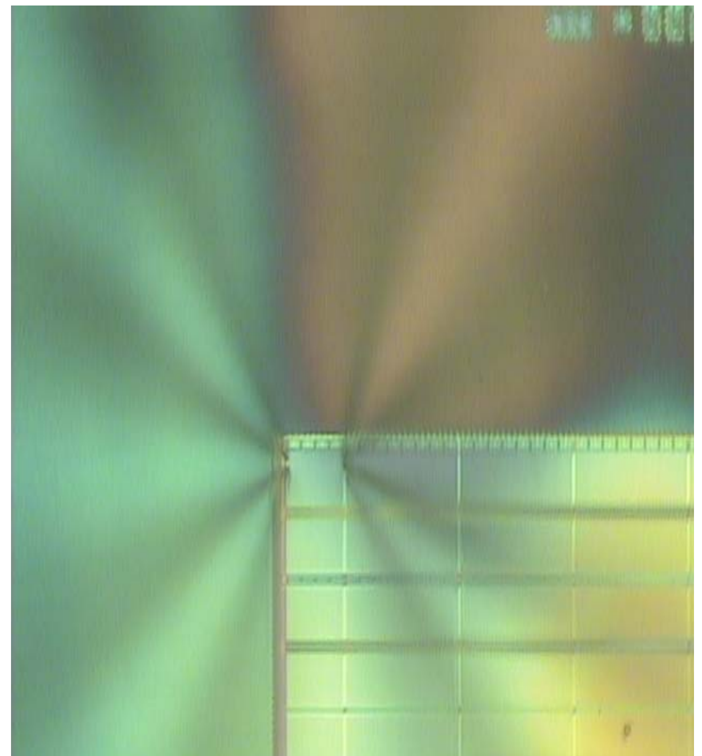

Figure 3a
Optical View of nanoprobes measuring an embedded DRAM cell. The two probes on the right are fixed, contacting wordlines. On the left, two nanoprobes are scanning simultaneously over the array of bitlines while maintaining the bit line pitch to check for trench leakage

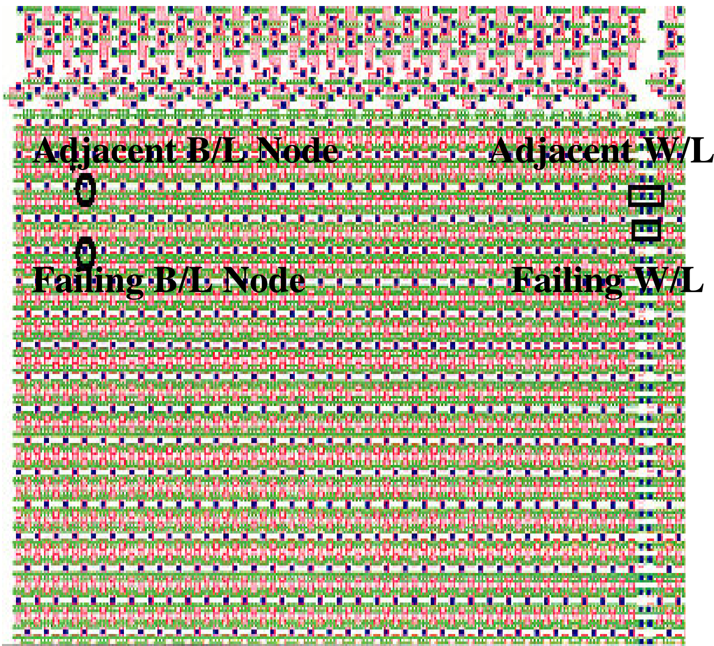

Figure 3b
CAD layout of the eDRAM array with the marked probing nodes of the word lines and bit lines corresponding to Figure 3a (above)

This means that at least two contacts must be involved in the process. It has become common practice to use one probe to contact a well or substrate contact and therefore create a path from one scanning probe to another fixed probe.[16, 17]
However, if in this case the leakage path is only between adjacent cells, no current can be collected from the bit line to the substrate. This is one difficulty of working with SOI. Figure 3a shows an optical image of a four probe DT leakage technique performed on a 65nm SOI eDRAM array.[16] Two probes on the right are stationary, contacting wordlines and holding them high. These are the wordline probes. Additionally, two probes (one of which is biased), are scanning an area on the array containing a trench to trench leakage defect. These are the bitline probes. The other bitline probes are scanned simultaneously maintaining exactly the same spacing as the bitline contact pitch. When the biased probe is scanned over a bitline contact, its grounded partner is contacting an adjacent bitline. Furthermore, the wordline probes activate the transfer device as shown in Figures 4 top, 4 middle, and 4 bottom.
The wordline probes also connect the BL's to their respective trenches.[16] This measurement was done on a portion of the array (chosen at a corner for clarity) and the resulting probe current image is shown in figure 5

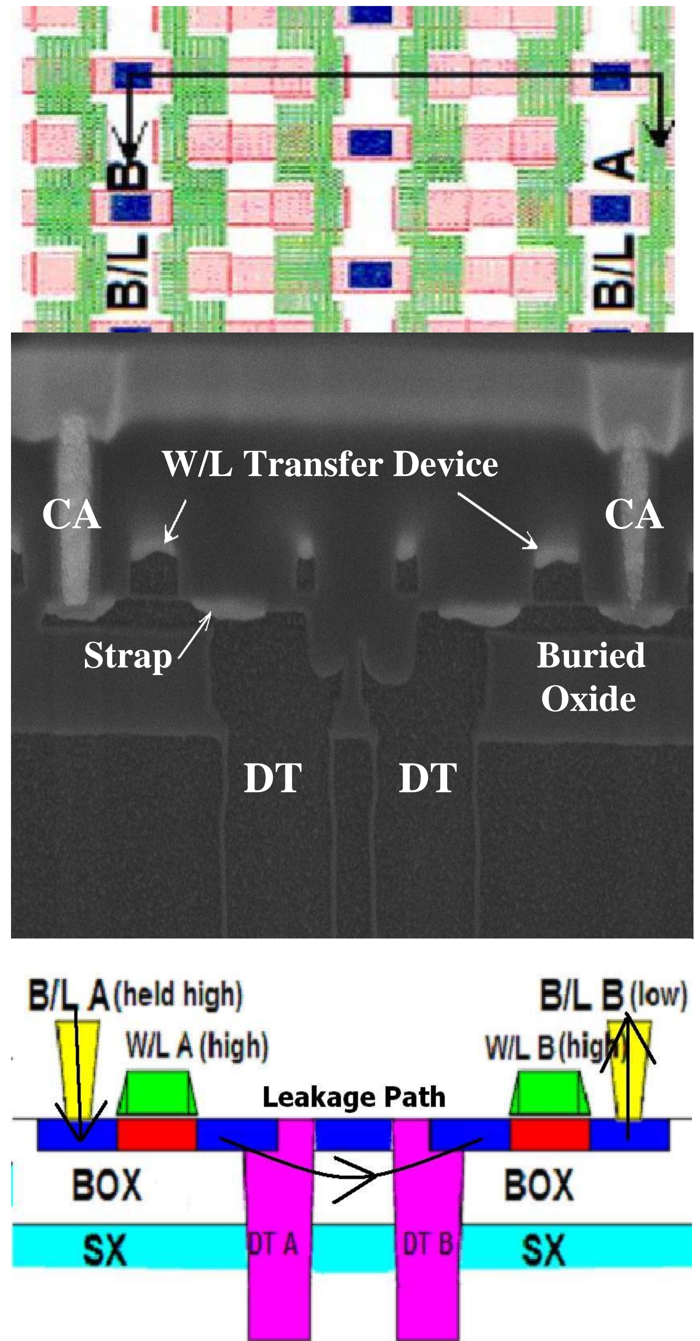

Figure 4
Top: Circuit layout showing the cross section orientation
Middle: SEM image of a FIB cross section through a representative DT set similar to the set that was measured electrically. The anomaly in the isolation between the trenches is not necessarily a failure. The tricky nature of finding a femto or pico amp leakage path between failing cells underscores the importance of nanoprobing analysis.
Bottom: A schematic of the leakage path measured between trenches. Note that the wordline blocks access directly to the DT capacitor. The wordlines must be both toggled high to allow access to the buried isolation.

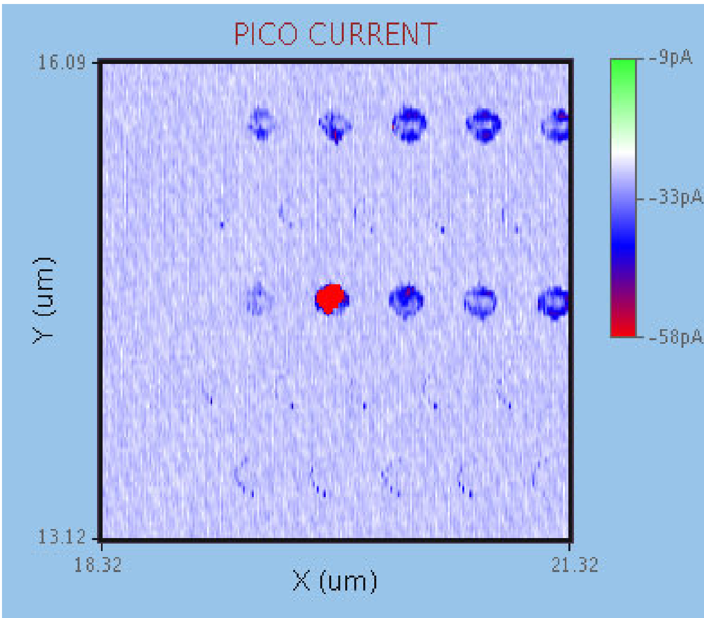

Figure 5
Current image showing leakage at failing bit line contact of leaky eDRAM cell corresponding to the layout shown in Figure 6 The current imaging is so sensitive that all of the bitlines adjacent to the contacted wordlines pass some current due to the leakage in the wordline gate oxide. But the trench that is leaking to its neighbor shows much higher current.

It is not possible to detect node to node leakage in an ordinary nanoprober without the unique simultaneous scanning feature except by painstaking checking of each pair of nodes.[16, 17]

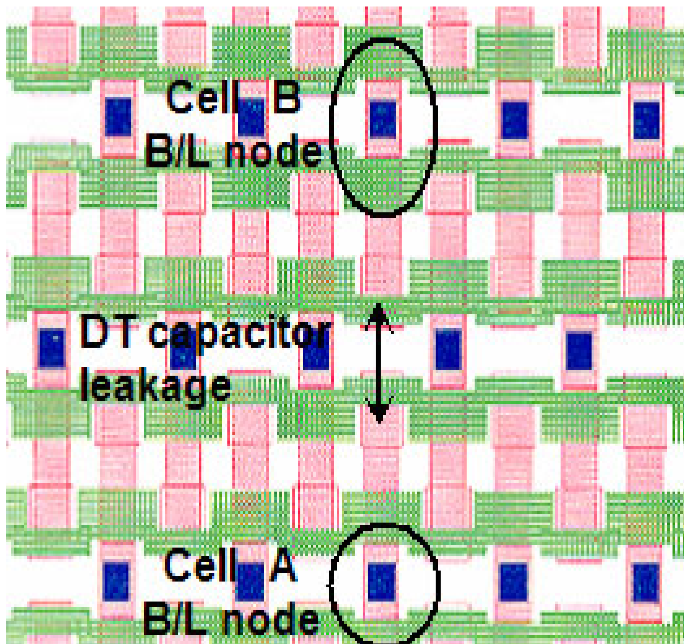

Figure 6
Detail of bit line nodes contacted during nanoprobing for deep trench capacitor leakage measurement between adjacent cells

Deep Trench Leakage IV measurements

Figures 4 and 6 describe the layout of these nodes. The eDRAM layout depicting bit line nodes and word line nodes employed in detection of deep trench capacitor leakage between adjacent cells is shown in Figure 4 bottom.
For the current leakage IV measurements, two probes contact the failing word line node and the adjacent word line node. Two other probes contact the bit line node in one cell and the bit line node in the adjacent cell .[16]
Nanoprobe current imaging of the adjacent bit line nodes revealed leakage between two adjacent cells. Figure 5 shows the current image. By contacting bitline A and bitline B and activating the corresponding wordlines, an electrical short is measured. Next, by toggling one of the word lines off, the deep trench capacitor is isolated from the bitline and no current flows as the voltage is swept positive. However as the bitline voltage sweeps negative, it crosses the threshold voltage of the wordline transfer gate and turns the transistor on so that the leakage current is again measured beyond the threshold voltage of this transfer gate device. The leakage must now be trench to trench and is not associated with either a wordline defect, substrate shorts or silicide pipes.

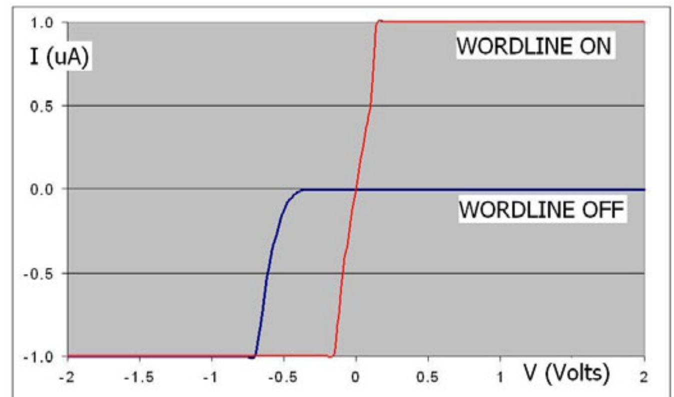

Figure 7
Two IV curves between Bitline contacts to failing (leaking) adjacent cells. Toggling the word line on connects BLA and BLB to the adjacent trenches (DTA and DTB), since there is a defect in the isolation between trenches, an electrical short was measured. With the wordline off, the Bitline A is disconnected from DTA and no current flows. The wordline transistor turns back on when the voltage on Bitline A is swept negative and the current resumes.

A correlation can be established between the nanoprobe current imaging signatures with subsequent electrically probed measurements. Validation of the current imaging signature is demonstrated by the resulting nanoprobing results and shows the importance of current imaging as a rapid inspection method for detection of defects in eDRAM cells.

Scanning Capacitance

The scanning capacitance microscope has become a staple in semiconductor metrology and failure analysis.[18, 19, 21, 22] Until now, it had not been available in conjunction with nanoprobing. The powerful combination of nano CV with nano IV should be a compelling improvement over either technique alone. In the case of SOI, capacitance imaging is evolving into an essential component. In Figure 8 below, scanning capacitance imaging over the eDRAM array yielded a bright contrast inspite of the fact that all contacts are electrically isolated from the substrate contact by the BOX layer. The BOX layer is invisible to the capacitance microscope because it sees the large BOX area capacitor in series with the much smaller device capacitor measured.

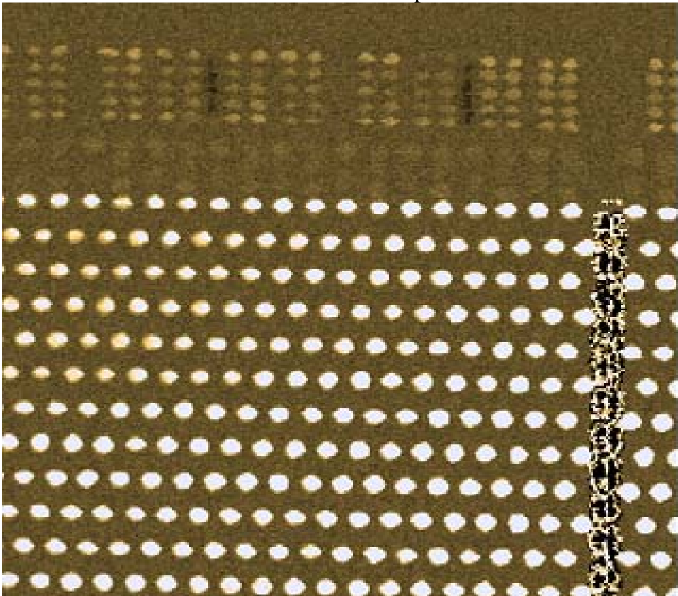

Figure 8 shows a scanning capacitance image of the eDRAM array, current imaging shows no contrast due to the presence of the oxide layer insulation.

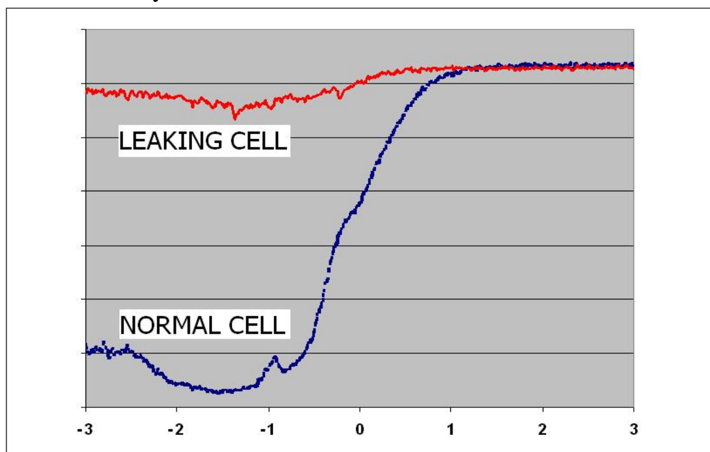

Figure 9
CV plot of the bit line contact node in the failing eDRAM cell (red plot) versus the bit line contact node in the non failing eDRAM cell. The Y scale is in femptoFarads and the X scale is in volts.

CV plots were taken with the newly designed capacitance sensor operating at 1 GHz. Without changing the tip following AFP current imaging or AFP probing results, the sensor used the same AFP tip to produce these results. An innovative resonator type design coupled with contact measurements enabled these measurements.

These plots exhibit depletion characteristics described in the literature.[18, 21, 22, 23]. The results have higher signal to noise relative to CV and dC/dV vs. V plots reported with the typical RCA style capacitance sensor.[24, 25]

The leaking DRAM cell's BL CV curve does not show depletion whereas all of the non-leaking cells gave virtually identical depletion curves. It can be assumed the leakage in the cell loads the depletion bias and therefore affects the curve. As the technique of scanning capacitance imaging with current imaging develops, it should prove to be an invaluable tool for fast defect location in eDRAM .

Conclusions

High performance Logic-based embedded DRAM based on the 65nm SOI platform have previously ben demonstrated with ~ 1.5ns latency and < 2ns random cycle cell characteristics.[1,-15]

These designs employing on-processor eDRAM overcome limitations in SRAM cache involving standby current, requirements for error correction circuity to address soft error rate (SER), and Vmin cell stability.[1,2] The challenges to nanoprobing and electrically characterizing discrete embedded DRAM cells (0.127 μm^2 for 65nm SOI designs and 0.067 μm^2 for 45nm SOI designs) in these embedded 2Mb caches and 4Mb caches are formidable. The demonstrated utility of nanoprobing current imaging to rapidly scan and detect defects in eDRAM cells coupled with complimentary scanning capacitance image capability offers a rapid means of identifying buried node leakages at contact (CA) level.

The possibility of early detection (at CA level) of FEOL defects offers the promise of localizing defects without the time consuming sample preparation steps employed in conventional PFA techniques.

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