

## Dislocation related Leakage in Advanced CMOS devices

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### Abstract

With high implant doses, strained silicon technologies and shrinking feature sizes, dislocation related failures seem to gain more importance in advanced CMOS devices. On the basis of case studies, different types of dislocations as well as the electrical characteristics of the corresponding devices will be presented.

### Introduction

Dislocations have long been known as a root cause for defects in semiconductors. Especially when they are crossing the p/n-junction of a device, leakage currents are a well known mechanism [1][2]. Regarding the formation and promotion of dislocations, process induced mechanisms have been identified as major contributor [3][4]. E.g. the ion implantation processes used for the formation of source, drain and well regions of CMOS devices. Unfortunately, these implantations are creating point defects and causes a lot of crystal damage [5].

Subsequent annealing steps are introduced to repair these damages, but still there is a chance for crystal defects to remain close to critical areas of the completely processed device. Especially high accumulated stress built up during the formation of the shallow trench isolation (STI), oxidation or gate stack formation promotes the formation of crystal defects [6].

The formation of stress induced dislocations is known to be a two step process. It starts with the nucleation of a dislocation loop which is the result of "precipitations" of the excess interstitial population that exists after ion implantation [7][8][9] followed by subsequent growth into critical regions of a device. Ion implantation, oxidation process steps and gate stack formation are major contributors to this behavior. With the aid of finite element simulations, the dislocation dynamics can be predicted for certain device structures [10][11]. In addition, the doping of the substrate increases the velocity of dislocations in comparison to undoped silicon [12].

Electrical characteristics of devices can be indirectly or directly affected by dislocations. They can change the point defect concentration around the loop layer by emitting [13] and capturing [14] interstitials, thus causing enhanced/retarded dopant diffusion.

In n-doped material, dislocations behave as acceptors. In p-type silicon they show a donor-like behavior [12]. This mechanism leads to the formation of a leakage path following the propagation of the defect. Hence, if a dislocation reaches into the p-n-junction of a device, it can increase the leakage current when it lies across the device junction [5] or finally result in the total electrical failure of a device [7].

In order to understand the mechanisms of the formation of dislocation as well as their influence on device characteristics, detailed imaging of these defects is essential. Methods like x-ray topography and chemical decoration are commonly used to show the positions and distribution of dislocations. But, these techniques have a major drawback for in depth analysis since they cannot give sufficient information about size, orientation or type of the defect.

The most effective tool for detailed analysis of dislocations and crystal defects is the transmission electron microscope (TEM). By using various operation modes like e.g. bright-field, dark-field or weak-beam imaging size, position and orientation of a dislocation can be determined. Imaging under various tilt angles can be employed as well as advanced preparation techniques [15] to get a 3-dimensional impression of the defect.

The objective of the work presented here is to make a link between the structural information about the defect and the electrical characteristics. Different types of dislocations characterized by their position, size, shape and orientation are correlated and with the resulting change in the electrical characteristics of affected devices. The electrical part of the analysis, curve trace measurements mainly on contact level, were used to get I-V curves for source-drain- or diffusion-well diode characteristics or leakages measurements, respectively.

## Case Studies

In the present work, three different types of dislocations are discussed: (i) long ranging dislocation dipoles, (ii) stress induced crystal defects and (iii) small dislocation loops.

### (i) Dislocation dipoles

The example for a long ranging dislocation dipole is from a device which failed due to increased pin leakage. In this case, the position of the fail was localized by backside emission microscopy as well as by TIVA. The position of the failing device was located within the ESD structure of the pad. Subsequent surface parallel delayering was performed to gain direct access to the failing device. After FIB pad deposition, the diffusion-to-well characteristic of the failing transistor was measured and compared to a reference. Figure 1 shows the ohmic leakage characteristic that was found for the affected diffusion.

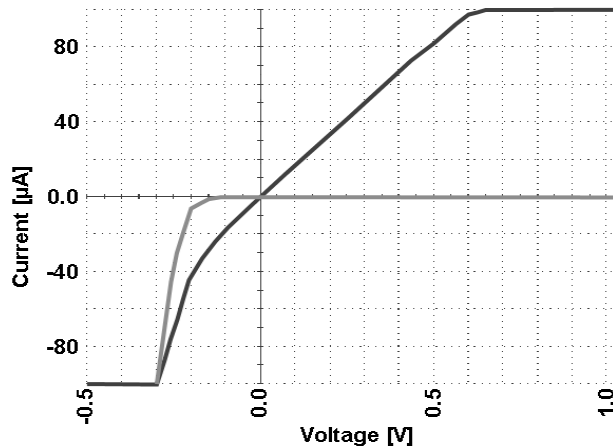


Figure 1: Diffusion-well characteristic generated by the dislocation dipole shown in figure 2. In this case, a relatively high leakage with an ohmic component in the zero-volt region was found.

After localization and electrical characterization, a plan view TEM sample of the area including the failing device was prepared. After total lift-off by wet chemistry, further preparation followed standard methods comprising mechanical polishing and subsequent ion-milling. Figure 2 shows the image from the localization as well as the corresponding TEM micrograph. In this case, two dislocation dipoles, each longer than 2 µm, were found right at the position of the TIVA signal.

After additional thinning of the sample, the more detailed bright-field and dark-field images in figure 3 show the exact position of the lower dipole. It was found that the upper end of the dislocation is reaching the top of the substrate in the gate area. Imaging at various tilt angles shows that the defect is inclined and reaching down towards the well. Due to the additional thinning, in figure 3 the lower end of the dislocation dipole is cut away, compared to the overview in figure 2.

Taking into account that along the propagation of a dislocation a leakage path is opened [1][4], one can easily link this defect to the measured IV-characteristic. In this case, the long ranging dislocation dipole reaches from the diffusion down to the substrate, thus opening the measured leakage path.

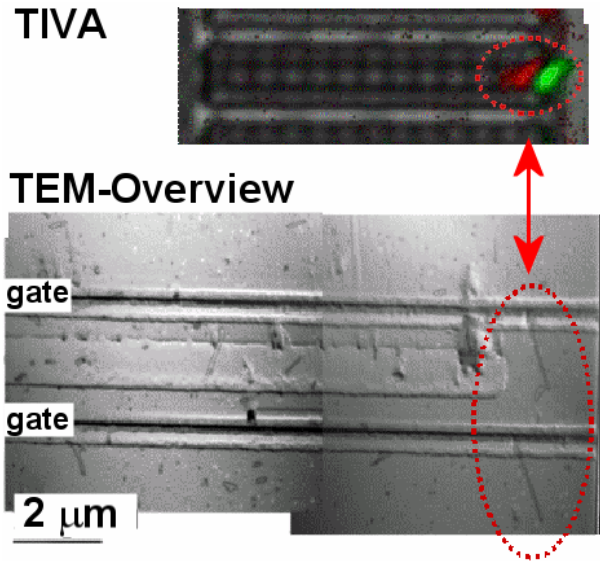


Figure 2: Plan view TEM image and the corresponding TIVA image (different scale) of the failing device. The localized TIVA signal directly corresponds to the position of the dislocations.

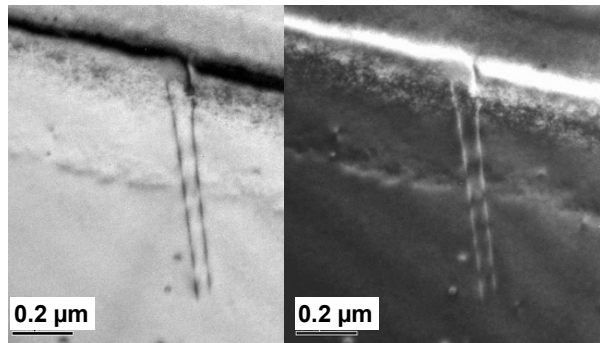


Figure 3: Detailed plan-view bright- and dark-field TEM images of the lower dislocation dipole shown in figure 2.

### (ii) Stress induces crystal defects

As an example for a stress induced defects, the second case study presents the analysis of single cell SRAM fail. In this case, no elaborated localization procedure was necessary, since the position of the defective cell is well known from descrambling the logic address of the failing bit. After surface parallel delayering to contact level, all transistors of the 6T-SRAM cell were characterized by measurements with the atomic force prober (AFP). As shown in figure 4, source-drain leakage was found for one n-FET within the SRAM cell.

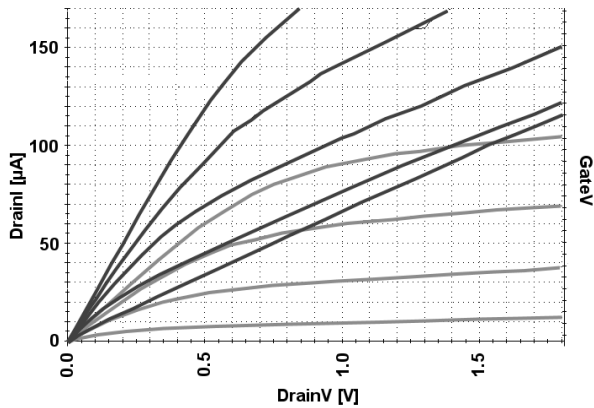


Figure 4: The dark lines correspond to the characteristics of the failing device (red line) shown in figures 8. In this case, the transistor shows source drain-leakage, while no leakage to the well was found. In comparison, the bright lines show the characteristics of a reference transistor.

Since no gate leakage was measured and the diffusion-well diodes were without any objection, a sample for TEM cross section imaging was prepared.

TEM cross section imaging of the failing transistor showed another typical type of crystal defect. As shown in figure 5, a dislocation crossing the device from source to drain was found. In order to estimate the position of the dislocation in y-direction, the sample was tilted around the z-axis. In figure 6 the sample was tilted by 25 degrees with respect to the edge-on orientation of the gate. It can be seen that the defect is crossing the channel at the level of the source / drain contact.

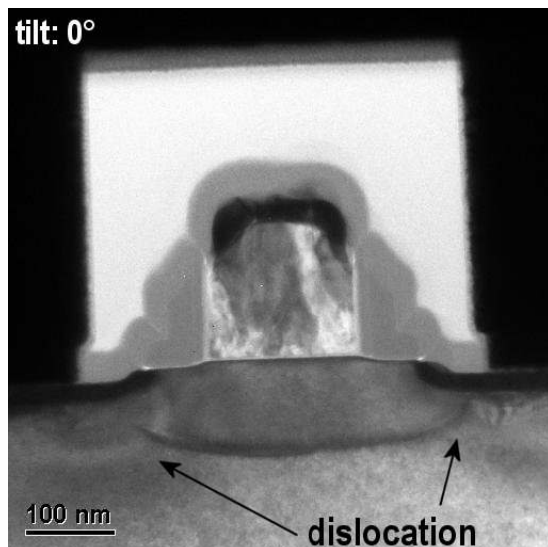


Figure 5: Cross section TEM image of a stress induced crystal defect imaged at 0° tilt angle. In this case the dislocation is spanning the device from source to drain.

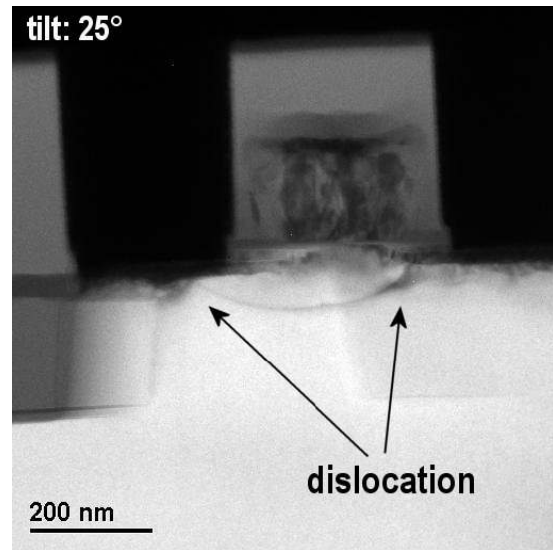


Figure 6: Cross section TEM image of a stress induced crystal defect imaged at 25° tilt angle. In this case the dislocation is spanning the device from source to drain.

In this case, it is assumed that locally built-up stress is the root cause for the generation of a defect at this specific position. Again, the dislocation induces a leakage path along its run which results in the leakage characteristic shown in figure 4.

### (iii) Dislocation loops

The third type of crystal defects discussed in this article are small dislocation loops. The case study selected as an example for this effect was coming up with a bit-line oriented failure in the diffusion-type read-only memory (ROM). Coarse localization of the failing cell was performed by backside emission microscopy. The position of the emission spot in combination with descrambling information from the known bit-line reduced the number of fail candidates to a few. After delayering to contact level, AFP measurements were carried out on the pre-selected contacts. An increased leakage from the diffusion contact to well was found for the failing ROM-cell in comparison to a reference. The corresponding IV-characteristics are shown in figure 7. In contrast to the other types presented, no ohmic component was found in this case. At lower reverse bias voltages, the current measured is still comparable to a good device. A minimum threshold voltage is needed to get sufficient leakage.

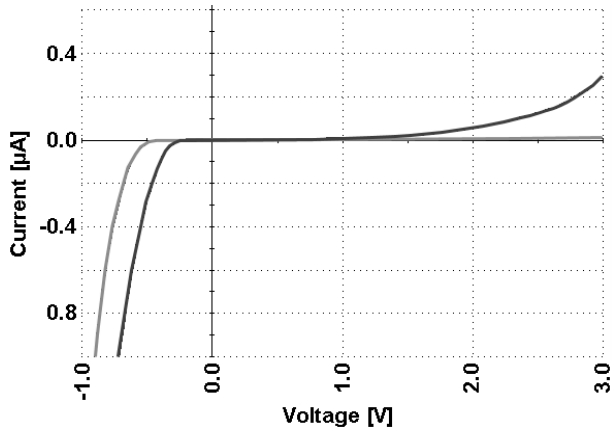


Figure 7: IV-characteristics measured from the central contact in figure 3a to well. The failing device (red line) shows reduced  $U_{th}$  and leakage in reverse bias.

By focused ion beam (FIB) lift-out technique, a TEM sample was prepared for cross-section imaging. The overview image of the failing device is shown in figure 8, where a small dislocation loop beneath the gate was found. More detailed bright and dark-field imaging in figure 9 reveals the position and the size of the dislocation. It is located a few nanometers beneath the gate oxide and has a maximum diameter of about 30 nm.

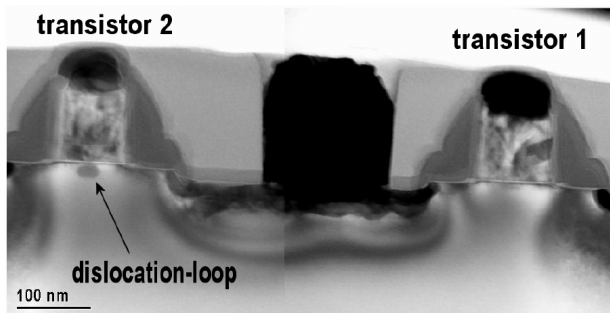


Figure 8: In this case, cross-section TEM imaging shows a dislocation loop in the channel of the failing transistor.

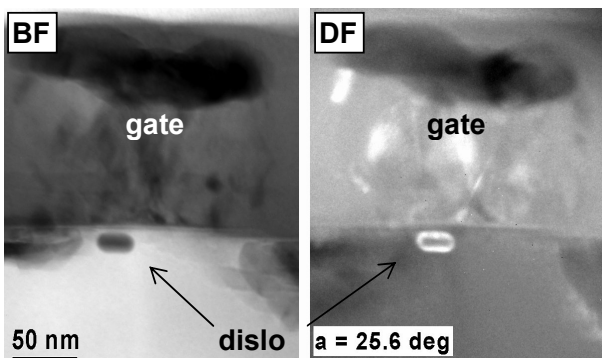


Figure 9: Detailed bright-field (BF) and dark-field (DF) image of the dislocation loop in the channel region. The size of the loop is  $\sim 30$  nm.

With the dimensions found, the dislocation cannot cross the channel of the FET completely. Again, assuming the leakage-path model along the defect, the resulting electrical characteristic in figure 7 can be explained. The effect of this dislocation is comparable to a shortened gate length, since the leakage path brings source and drain closer together. Finally, the electrical signature results in a reduced threshold voltage of the failing transistor.

## Discussion

In the case studies presented, three different types of dislocations were found in failing devices processed in advanced CMOS technologies. The dimensions of these defects are ranging from long, line shaped dislocation dipoles spanning several micro-meters to 30 nm dislocation loops. Comparing the morphology of the defects with the corresponding electrical characteristics, a consistent model can be proposed. The electrical behavior of the three cases can be explained by the assumption, that a leakage path along the propagation of the dislocation is created. This correlation is emphasized by the summary of the findings given in table 1. It shows how the type and the size of the defect are linked to the electrical characteristic of the failing device. Reading this table in the other direction, the type of defect can be deduced just from the electrical curve trace measurements.

## Conclusion

Based upon several case studies, the link between leakage path and defect position has been emphasized by electrical characterization and subsequent TEM imaging of failing CMOS devices. As summarized in table 1, this understanding of the correlation between the defect and its electrical footprint can help to classify and identify dislocations. Therefore, having a detailed electrical characterization of a failing device with respect to leakage paths and threshold voltages, a forecast of the type of defect responsible can be given. This understanding can help to reduce failure analysis turn around time. Especially, since it reduces the need to analyze dislocations by time consuming TEM analysis. The classification of the defect can be performed by standard curve trace measurements. In suitable cases, the identification of dislocations can even be performed with inline screening methods [16].

Table 1: Summary of the electrical characteristics compared with the type of dislocation found.

case	type of dislocation	defect size	I-V characteristic
i	dislocation dipole	$\geq 2 \mu\text{m}$	diffusion-well leakage
ii	stress induced, ranging from source to drain	$\sim 400$ nm	source-drain leakage
iii	dislocation loop in channel region	$\sim 30$ nm	reduced $U_{th}$ in reverse bias

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