

Investigation on the Influence of Focused Electron Beam on Electrical Characteristics of Integrated Devices

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Introduction

In recent years the application of nano probing systems has become widespread in semiconductor failure analysis. This is primarily due to the difficulties encountered in performing electrical characterization on latest technology nodes' integrated devices using standard probe stations (e.g. an optical microscope in combination with micrometer screw driven manipulators). Other reasons include the new capabilities offered by probing systems like current imaging and the growing rate of non visible or parametric fails.

There are two different types of systems available to electrically characterize devices at the contact level; one is based on the Atomic Force Microscope (AFM) platform and the other is a Scanning Electron Microscope (SEM) based system. The AFM based systems utilize several AFM heads (e.g. four heads to characterize one bulk transistor consisting of a gate, source, drain and corresponding well) equipped with conductive probe tips to map the sample surface in contact or non-contact mode. After scanning the area of interest, the probe tips are placed on top of the desired structure and a parametric analyzer extracts the data.

The SEM based systems are located in a high vacuum chamber and the sample surface is monitored along with the probe tip position by the SEM. These systems are also capable of positioning the probe tips on top of contacts or metal lines and it is possible to establish an ohmic contact to the device of interest.

For the SEM based systems it is known that there is an impact on certain device parameters like transistor I_{ON} and I_{OFF} which correlates to the primary electron beam acceleration voltage [1]. Nevertheless both types of systems are used in the semiconductor failure analysis community obtaining significant results [2, 3, 4].

Scope of this work

In the forefront of this work two questions arose:

1. Is it possible to use our SEM/FIB based probing system to do electrical characterization at device level

despite the fact that there is beam induced device degradation?

2. What are the effects to consider if a beam exposed sample has to be characterized by a nano probing technique during the failure analysis flow?

This leads to the concern for the optimum SEM conditions to avoid beam induced device degradation and the device parameters itself that are affected by beam radiation together with their dependency on SEM parameters.

To answer these questions the following experimental setup was employed.

Experimental Setup

As a representative device, a drive transistor (nFET) of a Single Port SRAM manufactured in a 90nm CMOS process was selected. The device parameters that were compared before and after the beam exposure were saturation current (I_{ON}), transistor leakage current (I_L), the subthreshold voltage (V_{TH}) and the slope (S). I_{ON} current is I_{DS} at $V_G=V_{DS}=1.2V$. The transistor leakage current I_L is defined as I_{SD} at $V_G=-0.3V$. V_{TH} values are obtained at $I_{DS}=8.25 \cdot 10^{-7}A$.

Before the experiments started, potential parameters having an effect on device characteristics such as beam acceleration voltage (V_{ACC}), beam dose (D); target device properties like height of the inter layer dielectric (h_{ILD}), gate oxide thickness (d_{GOX}), width (W) and length (L) of the transistor channel, and the materials used were identified. As an additional parameter, the time between the beam exposure and the re-characterization was taken into account.

In this work we present the results for different V_{ACC} levels and doses but not for the other parameters like height of the inter layer dielectrics, width and length of the transistor channel and the gate oxide thickness.

To characterize the devices electrically at the contact level before and after beam irradiation we assume that an AFM based system does not change device parameters. This was verified by several measurements of a transistor after deprocessing the sample to the contact level. No change in device characteristic could be observed after a series of measurements over a period of 2 days.

In the first step, a dependency of the device characteristics on SEM electron beam acceleration voltage (V_{ACC}) and electron

dose was investigated. To eliminate possible further influences the V_{ACC} and D scales were obtained from a separate die with the same preparation history and h_{ILD} across the SRAM cell array.

The doses used were: $1.6 \cdot 10^{-12} \text{As}/\mu\text{m}^2$ (D1), $1.6 \cdot 10^{-11} \text{As}/\mu\text{m}^2$ (D2), $9.3 \cdot 10^{-11} \text{As}/\mu\text{m}^2$ (D3), $4.7 \cdot 10^{-10} \text{As}/\mu\text{m}^2$ (D4), $2.8 \cdot 10^{-9} \text{As}/\mu\text{m}^2$ (D5). The dose values were calculated by multiplying electron beam current and exposure time divided by the affected (scanned) area.

The doses cover the range from a “just exposed by accident” level over slow scans used for imaging, up to high dose levels, i.e. high magnification coupled with long exposure time.

In the first experiment an acceleration voltage of 10kV was chosen. This is a commonly used setting for standard top down or cross section failure analysis tasks.

For the next experiments dose values were kept constant but the V_{ACC} was decreased to 5kV and 1kV.

To have an in depth look at the cause of the device parameter change, I-V characterization of the gate and source-drain regions as single components was performed. The goal was to determine possible changes in gate leakage currents and differences in the diode characteristics of the source-drain region to p-well.

Results and Discussion

Exposure of the nFET transistor at 10kV changes the device characteristic immediately and drastically (Fig.1a and 1b). It is clearly visible that even shortest exposure times (D1 equals 2s with a scanned area of $12 \times 12 \mu\text{m}^2$) lead to a significant change in I_L .

Besides the I_L , all other transistor parameters are changed as well. With increasing dose the V_{TH} shifts more than 300mV to higher values and the I_{DN} decreases by a factor of 4.5. The transistor slope S changed from 0.08V/dec up to 0.4V/dec for the highest dose.

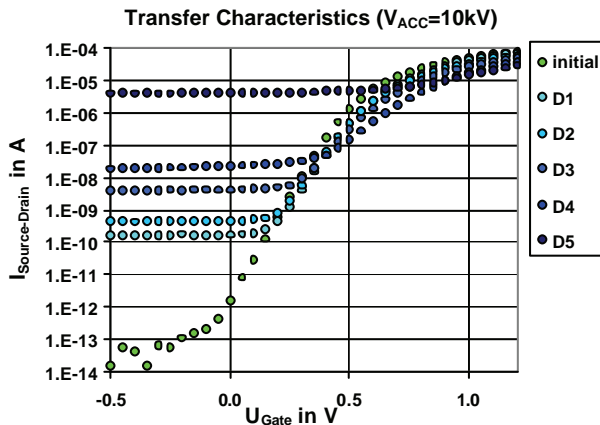


Fig.1a Input characteristics of the transistor at $V_{ACC}=10\text{kV}$ and different doses plotted in logarithmic scale.

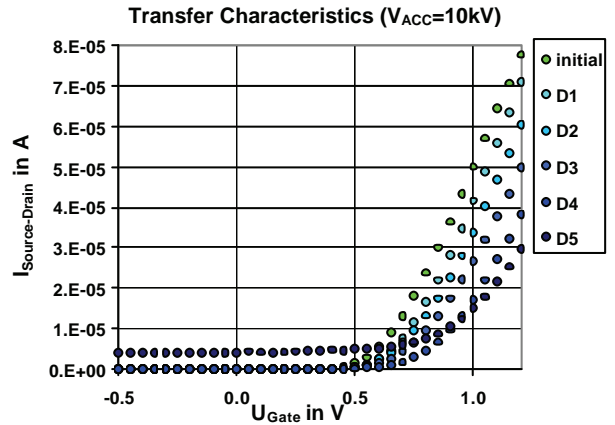


Fig.1b Input characteristics of the transistor at $V_{ACC}=10\text{kV}$ and different doses plotted with a linear scale.

These facts are an important issue for standard SEM analyses followed by nano probing device characterization. Compared to a non-exposed reference transistor, it is most likely that a single exposure of the electron beam on the target cell will lead to significantly altered device characteristics caused by the irradiation of the electron beam. Possible device failures might become masked due to the strong effect of the electron beam exposure.

In addition to the transistor I-V curves, gate leakage current to the underlying pwell and diode characteristics of the source-drain region to pwell were obtained.

Comparison of gate leakage currents shows increasing leakage values for higher doses D (Fig. 2). This might be due to gate oxide degradation as a consequence of trapped electrons or the creation of electron hopping paths due to the electron bombardment.

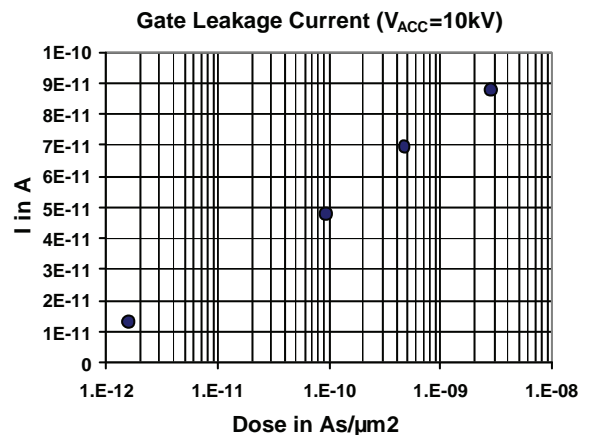


Fig.2 Increase of gate leakage with increasing dose of radiation.

Analysis of the source-drain region to pwell diode shows that an increase in the applied dose affects the resistance and leakage currents such that both values are increased (Fig. 3).

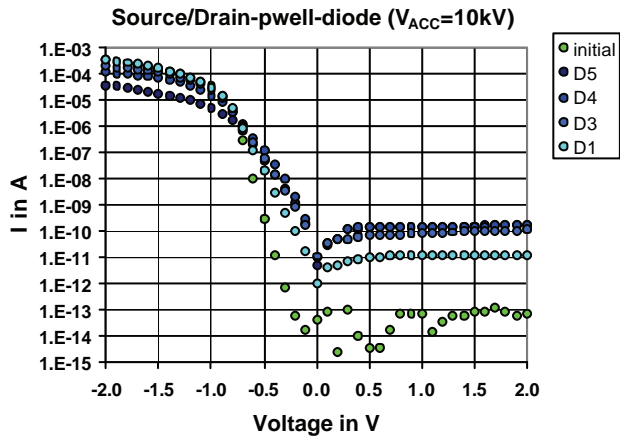


Fig.3 Resistance and leakage current of the source region to pwell diode increase with a higher applied dose.

For the lower beam acceleration voltages used in our experiments these effects are reduced drastically. Unfortunately it was not possible to avoid electron beam induced device characteristic change for all of the doses that were applied. For the worst case scenario (D5) device degradation could be observed even at $V_{ACC}=1kV$.

The trend charts are shown in Figs. 4a to 4d.

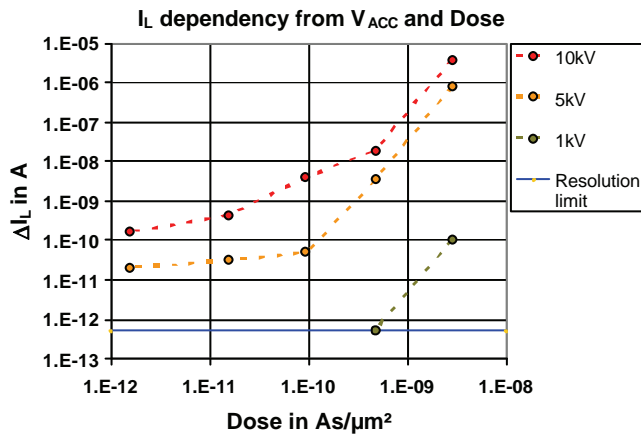


Fig.4a Leakage current I_L increases strongly with V_{ACC} and D.

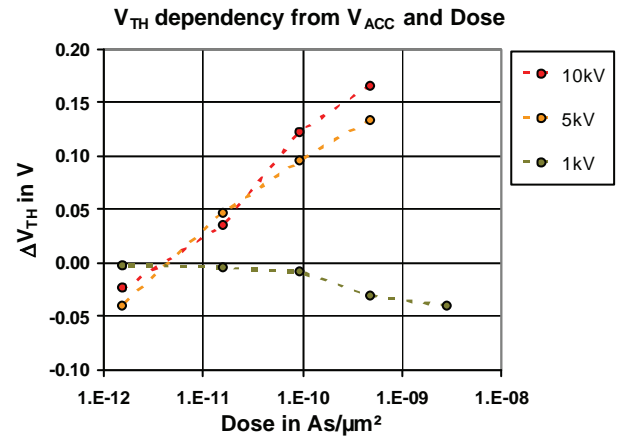


Fig.4b V_{TH} decreases slightly for $V_{ACC}=1kV$ and very small doses at higher V_{ACC} . High doses and high V_{ACC} cause an increase of V_{TH} .

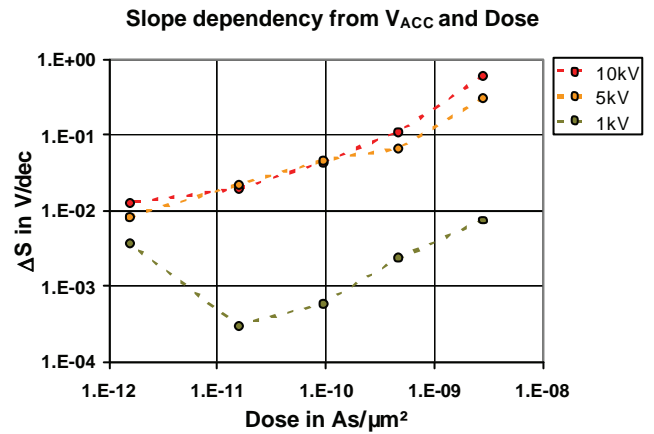


Fig.4c Slope S increases after electron beam irradiation. The initial slope is $8 \cdot 10^{-2} V/dec$.

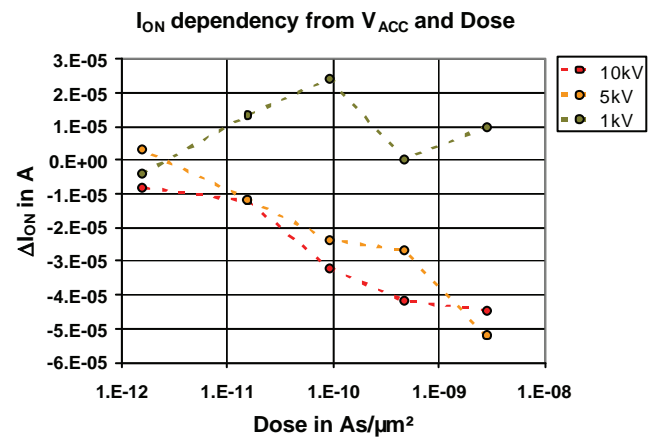


Fig.4d I_{ON} current decreases for 10kV and 5kV V_{ACC} .

Additional measurements with time intervals of one week and one month between exposure event and subsequent re-measurement of the transistor showed nearly no changes in the electrical characteristics.

Summary

Our data confirm the effect of electron beam induced alteration on integrated devices. It has been shown that several parameters influence the investigated device, e.g., beam acceleration voltage and dose used for radiation. It is also shown that several device parameters are affected. Differences in the unexposed transistor are evident for I_L and I_{ON} as well as V_{TH} and slope. While device leakage currents increase with higher exposure, the I_{ON} values decrease. The V_{TH} values shift to higher values for V_{ACC} values of 5kV and 10kV if doses higher than $1 \cdot 10^{-11} \text{As}/\mu\text{m}^2$ are applied. Otherwise ($V_{ACC}=1\text{kV}$ or D1 applied) the V_{TH} shifts to smaller values.

There are several publications available explaining the effects seen in our experiments [5, 6, 7, 8]. All of the explanations propose two main contributors to the device alteration.

The first one is trapped charge located in the gate oxide. The positive charge up of the gate should lead to a shift of V_{TH} in negative direction. This seems to be the dominant mechanism for older CMOS technology nodes [9].

The second contributors are electrons trapped in interface states. From our data it appears that for 10kV and 5kV acceleration voltages, this is the main culprit responsible for changes in device characteristics. For $V_{ACC}=1\text{kV}$, V_{TH} slightly decreases, indicating that the effect of the trapped gate oxide charge is dominant. From our point of view it might also be possible that charge is trapped in the interlayer dielectric. That would explain the different behavior at $V_{ACC}=1\text{kV}$. With the much shallower penetration depth at these low energies, the electrons are only trapped in the ILD, and do not reach GOX or bulk to GOX interface.

A decrease in I_{ON} currents might be also explained by an increase of the resistance of the source drain regions either to the underlying nwell or to the connecting source-drain contact. Diode characteristics of the source drain contacts to the nwell support this hypothesis.

In conclusion and as an answer to our initial questions it is possible to state that measurements with our available SEM based prober are possible, but under certain SEM conditions, i.e., low V_{ACC} and low doses. Only under these conditions, the electron beam influence on electrical device parameters such as I_{ON} , I_L , and S is negligible in most failure analysis cases. Special applications like signal margin fails due to slightly misaligned V_{TH} values of two transistors in the sense amplifier require a reliability to V_{TH} values better than 20mV. In this case it is important to operate the SEM at low accelerating voltages and simultaneously limit the dose applied to the device.

Our studies also show that it is critical to know the sample history before electrical device characterizations are carried out since electron beam induced device parameter changes are nearly unaltered over a long period of time after beam exposure.

References

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