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Combining the Nano-Probing Technique with Mathematics to Model and Identify Non-Visual Failures

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Abstract

In this paper, we focus on how to identify non-visual failures by way of electrical analysis because some special failures cannot be observed by SEM (scanning electron microscopy) or TEM (transmission electron microscopy) even when they are precisely located by other analytical instrumentation or are symptomatic of an authentic or single suspect. The methodology described here was developed to expand the capabilities of nano-probing via C-AFM (conductive atomic forced microscopy), which can acquire detailed electrical data, and combining the technique with reasoned simulation using various mathematic models emulating all of the significant failure characteristics. Finally, a case study is presented to verify that such defect modes can be identified even when general PFA (physical failure analysis) cannot be implemented for investigating non-visual failure mechanisms.

Introduction

With the evolution of advanced process technology, failure analysis has become more and more difficult because there are more erratic defect types arising from more non-visual failure mechanisms. For overcoming such difficulties in failure analysis, nano-probing can be enhanced in order to acquire more detailed electrical information before the implementation of PFA (physical failure analysis) [1].

In this paper, we focus on how to solve non-visual failures which cannot be observed by SEM or TEM even if they have been located by nano-probing via C-AFM and an authentic or single suspect was indicated via measuring and electrical analysis. In order to overcome the difficulties of failure analysis for such non-visual failures, a mathematic model for specific failure simulation is proposed to explain those characteristics impacted after electrical measurement data is extracted by nano-probing.

Case Study and Experimental

In order to explain our methodology and the related mathematical modeling, a typical single-side, blocked LDD (lightly doped drain) implantation case study is presented to demonstrate our novel method for applying electrical analysis to identify non-visual failures. This case study is chosen because the LDD implantation issue is notorious as a chronic problem for PFA experts.

First, let's begin with the measured data from the nano-probing of a failed transistor. As shown in Fig. 1, the failed transistor exhibits a smaller saturation current and an asymmetric behavior between the forward and reverse biased I-V curves.

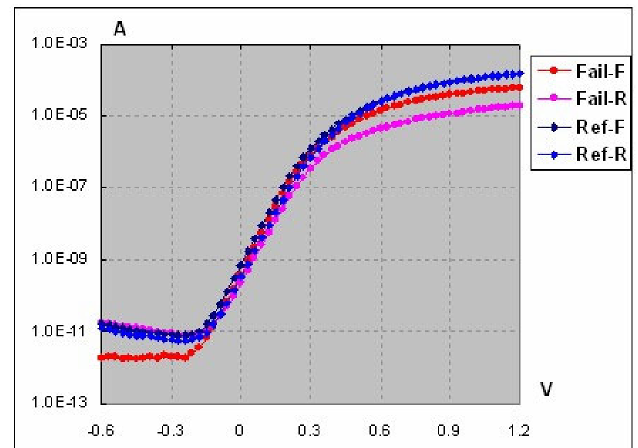

Figure 1: Comparison of forward (F) / reverse (R) Id-Vg curves for a reference and a failed NMOS when $V_D=V_G=1.2V$. Note the smaller drift current and asymmetrical behavior of the failed transistor test sweeps.

Because of the smaller drift current, a high-resistance issue was the first idea to arise as a cause. But, considering the inconsistent junction characteristics at both the drain and source of the failed NMOS, there was no obvious difference in the slope of the forward bias and this cause can be excluded (*Figs. 2 and 3*).

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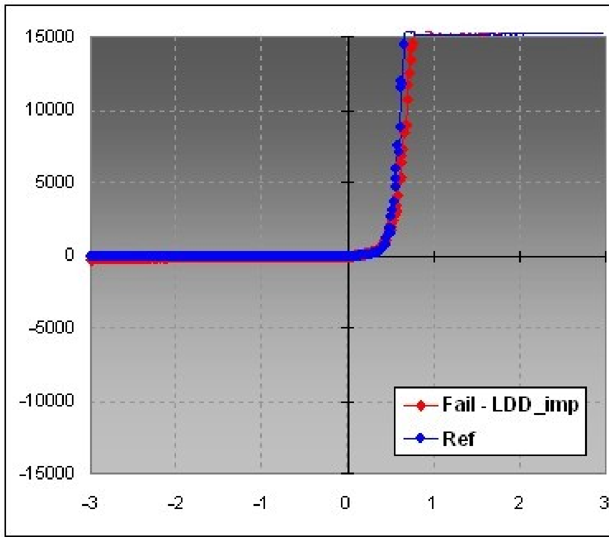


Figure 2: Quasi C-AFM I-V curve to check the junction characteristic at the drain/source of the failed NMOS. indicating no high-resistance issues at the drain/source.

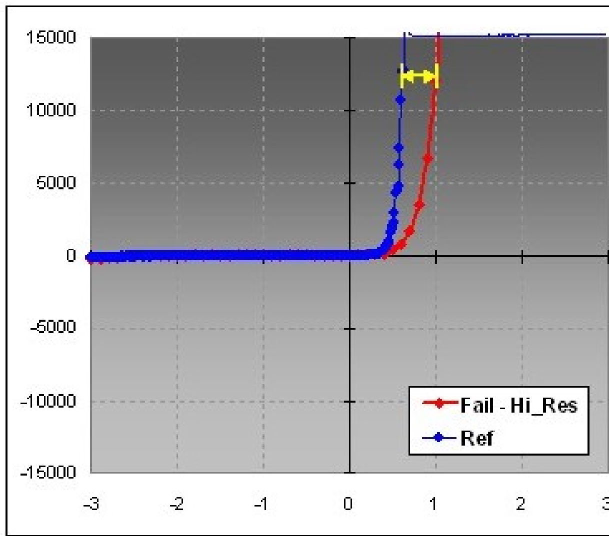


Figure 3: A typical high-resistance issue at the drain/source was verified by a quasi C-AFM I-V curve. (Please notice the forward-bias part of the I-V curve.)

Following this, the related implantation issues, which may impact the carrier intensity of the source/drain or the threshold dose of the channel, were highly suspect. Accordingly, based on our previous study of such non-visual implantation issues [2], these I-V curves and the unusual P-N junction characteristics could be produced and explained by the "ideal diode equation" and the "theory of the junction".

The ideal diode equation is given by:

$$I_S = J_S \times A \times (e^{qV/kT} - 1) \quad \textbf{(1)}$$

$$J_S = [\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}] \times n_i^2 \quad \textbf{(2)}$$

where

I_S : *reverse saturation current*

J_S : *reverse saturation current density*

A : *interface area of P-N junction*

V : *applied voltage*

D_p : *diffusion constant of hole*

L_p : *diffusion length for hole*

N_D : *N+ donor doping concentration*

D_n : *diffusion constant of electron*

L_n : *diffusion length for electron*

N_A : *PW accepter doping concentration*

n_i : *intrinsic concentration*

.

First, considering the above equations, since the value of the delta of the reverse saturation current density, ΔJ_S, is inversely proportional to the N+ doping concentration, N_D, if the PW concentration, N_A, is kept constant then the leakage current of this P-N junction is commensurate with the reverse-biased current, ΔI_S, and it should increase as the N+ implant concentration decreases accordingly. But considering the inconsistent result of the corresponding C-AFM measurement, there was neither larger leakage current when reverse biased nor a smaller cut-in voltage when forward biased. Thus, the suspected N+ implantation issue can also be excluded (*Figs. 2 and 4*).

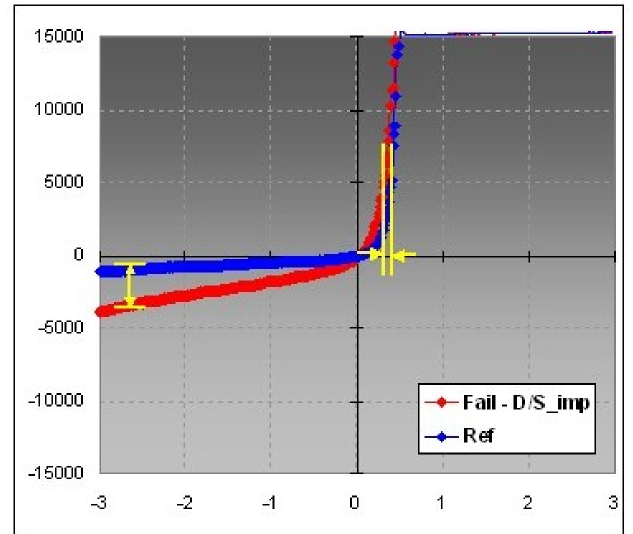
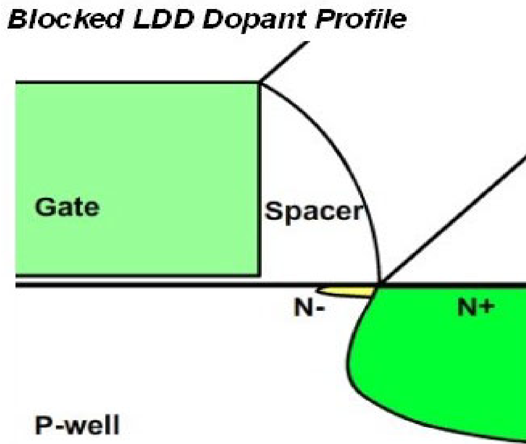


Figure 4: Typical N+ implantation issue at the drain/source was verified by a quasi C-AFM I-V curve. (Please notice the off-state current on the reverse-bias side and the cut-in voltage of the equivalent diode on the forward-bias side)

Consequently, after more deduction, a blocked LDD implantation was the most reasonable failure mechanism that fit our reasoning. (*Fig. 5*)

(a). Failed NMOS



(b). Reference NMOS

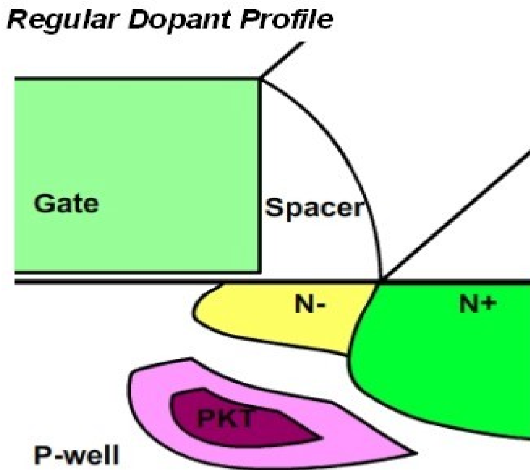


Figure 5: Comparison of the dopant profiles of a blocked LDD implantation and a reference NMOS. A conductance channel under the gate would be disconnected at the drain/source site.

Next, for satisfying the previous deduction due to the lack of physical evidence, the equivalent mathematic models were applied to describe the corresponding electrical I-V curves of the target MOS (metal-oxide-semiconductor) transistor. (*Figs. 6 and 7*)

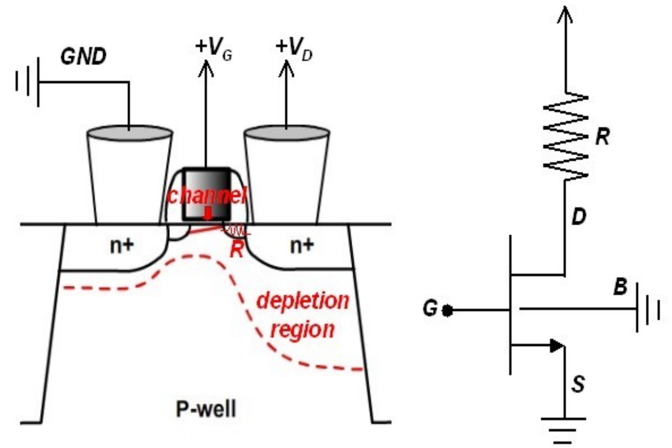


Figure 6: The missing LDD at the drain can be modeled as a smaller resistor because of a masked effect in the depletion region.

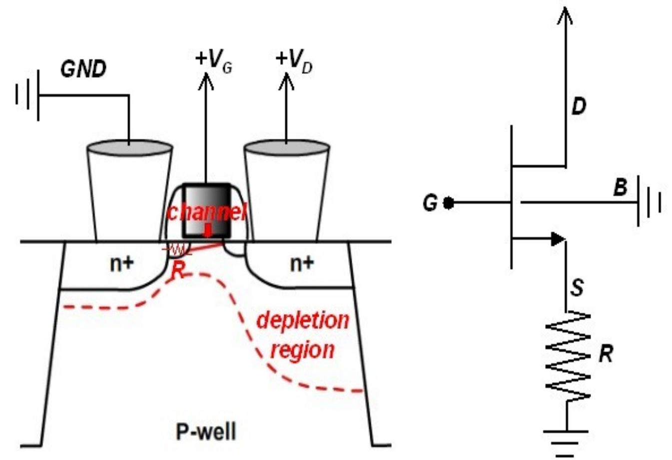


Figure 7: The missing LDD at the source can be modeled as a larger resistor because there are dual voltage drops in both the disconnected implantation region and the pinch-off site.

In most applications, more determinable electrical analysis for the corresponding mathematical models would consider specific theories or characteristic equations from semiconductor physics. Thus, with a view to MOS technology, the ideal equation for drift current operated in linear and saturation regions can be described as follows.

If $V_{DS} \le V_{GS} - V_{th}$,

$$I_D = \frac{1}{2}\mu \cdot C_{OX} \times (\frac{W}{L}) \times [2(V_{GS} - V_{th}) \times V_{DS} - V_{DS}{}^2] \quad \textbf{(3)}$$

If $V_{DS} \geq V_{GS} - V_{th}$,

$$I_D = \frac{1}{2}\mu \cdot C_{OX} \times (\frac{W}{L}) \times [V_{GS} - V_{th}]^2 \quad \textbf{(4)}$$

where

V_{DS} : *Drain-Source voltage difference*

V_{GS} : *Gate-Source voltage difference*

V_{th} : *threshold voltage of MOS*

I_D : *drift current of MOS*

C_{OX} : *Gate capacito*r of MOS

W : *channel width of MOS*

L : *channel length of MOS*

Considering that the MOS behavior of such a failure mode was related to a body effect and the source voltage, the threshold voltage of the transistor should become:

$$V_{th} = V_{t_0} + \gamma \times (\sqrt{2\Psi + V_{sb}} - \sqrt{2\Psi}) \quad \textbf{(5)}$$

where

V_{th} : *threshold voltage*

V_{t_0} : *threshold voltage without body effect*

V_{sb} : *Source-Body voltage difference*

Then, let's insert a single-side blocked LDD failure, the V_{GS} part would vary with the failure located site and the V_{DS} part would divide as:

$$V_D = V_{D1} + V_{D2} + V_{D3} \quad \textbf{(6)}$$

$$V_D = V_{D1} + V_{DS} = I_D \times R + V_{DS} \quad \textbf{(7)}$$

where

V_{D1} : *voltage drop at the disconnected LDD*

V_{D2} : *voltage drop at the channel*

V_{D3} : *voltage drop at the pinch-off site*

In general operation, the forced V_{DS} is equal to the biased V_D and the forced V_{GS} is equal to the biased V_G. But according to previous hypothesis, V_{DS} was only the parts of V_{D2} and V_{D3}, and V_{GS} was a variable dependent on such blocked LDD implantation impacted on the drain or source site.

Therefore, according to the corresponding mathematic models and representative equations, the resulting numerical analysis illustrates how such a failure mechanism can affect the abnormal NMOS characteristics and induce an asymmetrical behavior on the malfunctioning transistor (*Figs. 8 and 9*).

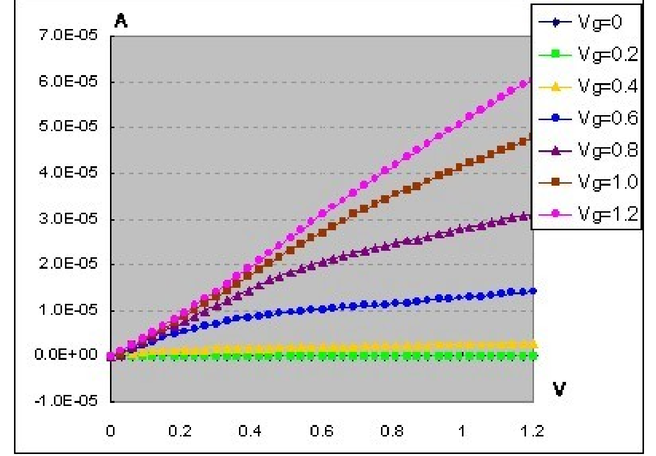


Figure 8: According to the above equations, if the missing LDD is at the drain site, an increasing I_D would cause a decreasing V_{DS} and make the linear region of the MOS expand to all ranges.

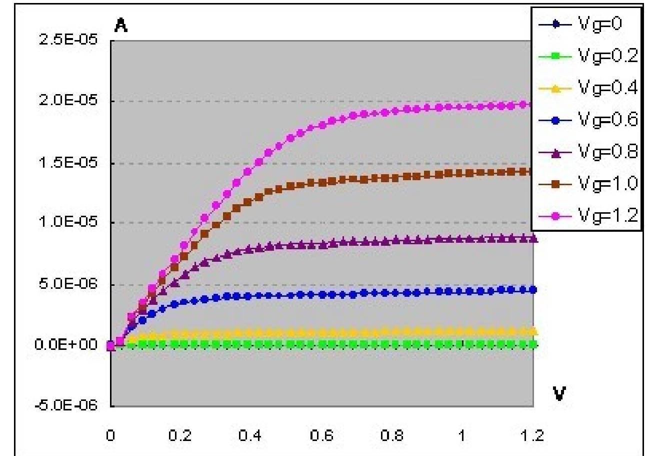


Figure 9: According to above equations, if the missing LDD is at the source site, although the pinch-off condition could be forced along, the dual shrinking factors of V_{GS} and V_{DS} still result in a very small drift current for the MOS.

Finally, some related PFA images are presented to validate our ratiocination and methodology. The discovered failures suffering from the non-visual implantation issue was verified by visual residual particles or associated artifacts from the wafer process although physical essence of the blocked LDD implantation was still non-visual via TEM observation. Thus, the application by means of electrical analysis that combines the nano-probing technique with mathematic modeling was

demonstrated to be an effective tool for identifying non-visual implantation issues and other related, unperceivable defect modes. (*Fig. 10*)

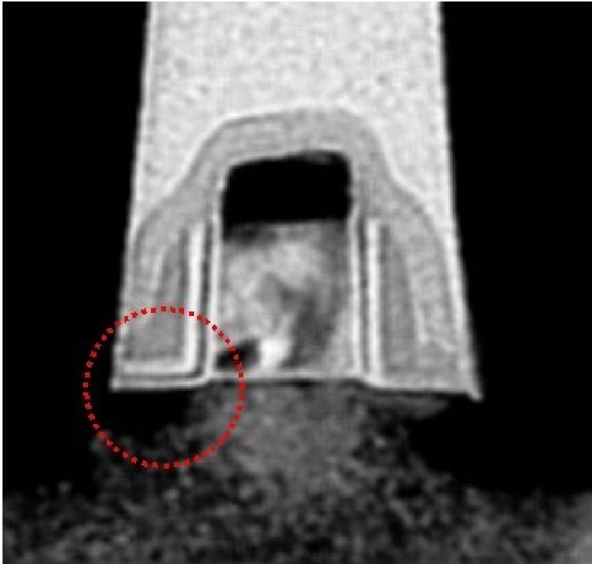


Figure 10: A typical example of an LDD implantation issue which was verified as a residual particle or visible artifact from the wafer process although the actual missed implantation region was non-visual to SEM and TEM.

Conclusions

At present, the nano-probing technique is a powerful tool for electrical characterization of a device. In this paper, the utilization of nano-probing was enhanced in order to acquire more complete electrical information before conducting definitive PFA. Also, the LDD implantation issue could be explained by exclusive methodology and mathematical modeling. Finally, the application of numerical analysis can be used to illustrate the impacted characteristics of the MOS.

References

[1] Cha Ming Shen, Tsan Chen Chuang, Chen May Huang, Shi Chen Lin, and Jie Fei Chang, "Coupling C-AFM with Nano-probing Technique for Further Junction Leakage Analysis", *ISTFA 2006*, pp. 167 - 171.

[2] Cha Ming Shen, Shi Chen Lin, Chen May Huang, Huay Xan Lin, and Chi Hong Wang, "Couple Passive Voltage Contrast with Scanning Probe Microscope to Identify Invisible Implant Issue", *ISTFA 2005*, pp. 212 - 216.