

## Analysis of DC Failure in Advanced Memory Devices Using Nanoprobing and Scanning Capacitance Microscopy

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### Abstract

This paper discusses the failure analysis process of a DC failure using an in-FIB (Focused Ion Beam) nanoprobing technique with four probes and a scanning capacitance microscope (SCM) in advanced DRAM devices. Current-Voltage (I-V) curves measured by the nanoprobing technique indicate the curve of the failed device is different from that of the normal device. The failed device causes a high leakage current in the test. The cross-sectional 2-D doping profile of SCM verifies the region of the P-Well has shifted to create a leakage path that causes this failure.

### Introduction

The DC test that is used to detect the external functionality of modern memory chips is one of the testing sequences during electrical testing of memory in wafer sorting. The output leakage current can be measured by applying appropriate DC voltages to each pin. Figure 1 is a schematic diagram showing the output leakage current that is measured in the test. To start this test, all the I/O pins are set at floating status. Then the voltages of  $V_{DDmax}$  and ground (GND) are applied to two power supply pins,  $V_{DD}$  and  $V_{SS}$ , respectively. The output leakage current can be measured by applying the voltages of  $V_{DDmax}$  or 0 to each of the output pins (DQ), while all other pins are grounded. If the pin is applied to the voltage of  $V_{DDmax}$ , the leakage current measured is called an " $I_{LOH}$ ". If the pin is applied with the voltage of 0, the leakage current measured is called an " $I_{LOL}$ ". Once the value of the measured leakage current is out of production specification, the chip is scrapped for further operations.

A nanoprober combined with either a scanning electron microscope or a focused ion beam system is used for electrical characterization of integrated circuit for failure analysis or for testing device quality in the semiconductor industry [1]. In general, incorrect implantations will cause the failures in semiconductor devices. As is well known, scanning capacitance microscopy (SCM) allows for the visualization of the 2-D implantation doping profiles in actual semiconductor devices [2-3]. Therefore, once a failure site location of the

specific device is confirmed by the nanoprobing technique, further SCM analysis can be employed to identify the physical causes on the device structures.

In this paper, we describe the failure analysis process which combines an in-FIB nanoprobing technique with SCM by using a specific case with advanced memory devices. The device that is failed due to a high output leakage current in the DC test is confirmed by nanoprobing for further verification of the physical cause by SCM.

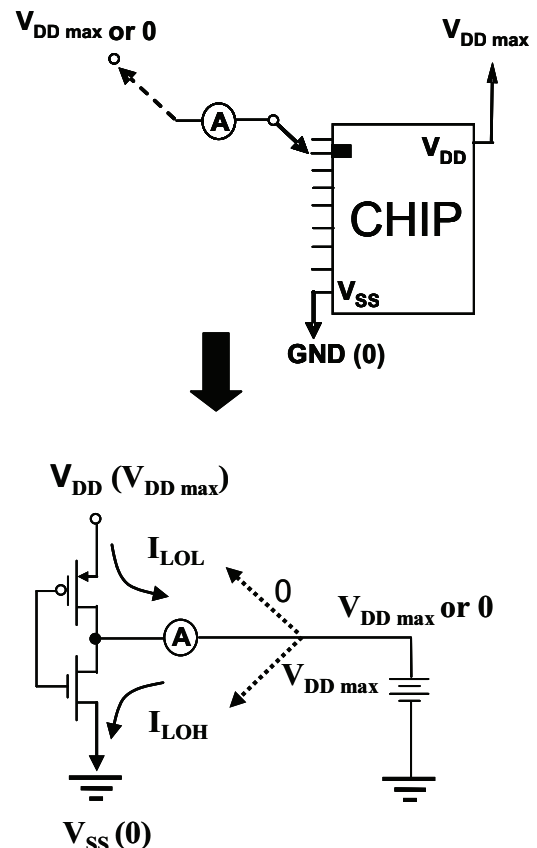


Figure 1: A schematic diagram showing the output leakage currents that are measured in the test.

## Problem Description and Failure Analysis

In our specific case, one advanced 512 Mega-bit DRAM wafer was failed due to a high output leakage current ( $I_{LOH}$ ) in the DC test of the final production test. The WAT (wafer acceptance test) data on the test structure that monitors the electrical characteristics of low  $V_t$  (threshold voltage) P-MOSFET (PMOS) in the SA (sense amplifier) circuit showed the measured  $V_t$  is out of specification. Although the failure in the SA circuit did not contribute to that in the output circuit, analysis of the failure in the SA device was done to understand if there is any hint for the failure of the output circuit.

There are two PMOSs designed in the test structure for low  $V_t$  PMOS of SA. The WAT data indicated that one PMOS has failed, but another one is normal. This information provides a comparison between the normal device and the failed device for further nanoprobeing and SCM analysis.

Nanoprobeing was employed in a FEI FIB 200 system with a Kammrath & Weiss prober-module. The SCM images of the 2-D doping profiles of the desired device structures were obtained using a commercial DI-3100 Atomic Force Microscope (AFM) equipped with a SCM application module. A 0.5V AC bias at 90 KHz and a 0.0V DC bias between the conductive tip and the sample were used for this analysis.

The failed chip was polished to the contacts level for the source (S), drain (D), gate (G) and bulk (B). The probing tips were then applied to the contacts. The source voltage, the drain voltage and the bulk voltage were set to simulate test conditions of WAT. The  $I_D - V_G$  curves of the normal and failed devices were then measured by ramping down the gate voltage from 0.5 V to -2.0 V (Fig. 2). The curve of the failed PMOS device has shifted to the right side of that of the normal PMOS device. The failed device has a high current at a lower gate voltage. This result indicates that there is a leakage path in the regions of source or drain.

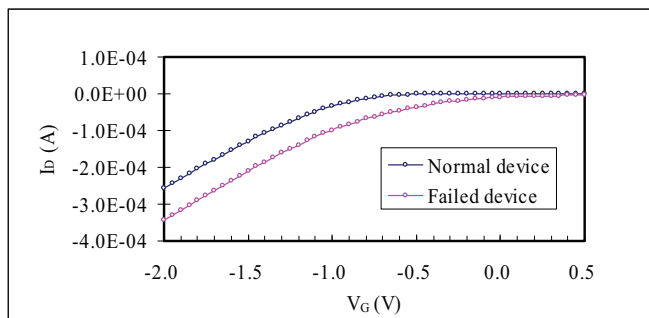


Figure 2:  $I$ - $V$  curves showing the differences between the normal device and the failed device.

Figure 3 shows the cross-sectional SCM images of the normal and failed PMOS devices. The drain region is isolated by STI (shallow trench isolation) from the region of the P-Well in the

normal device. However, the region of the P-Well bridges the drain region in the failed P-MOS device that causes a leakage path of high current in the electrical test. This abnormality is caused by the shift of the photo mask on the implantation of the P-Well during the manufacturing process.

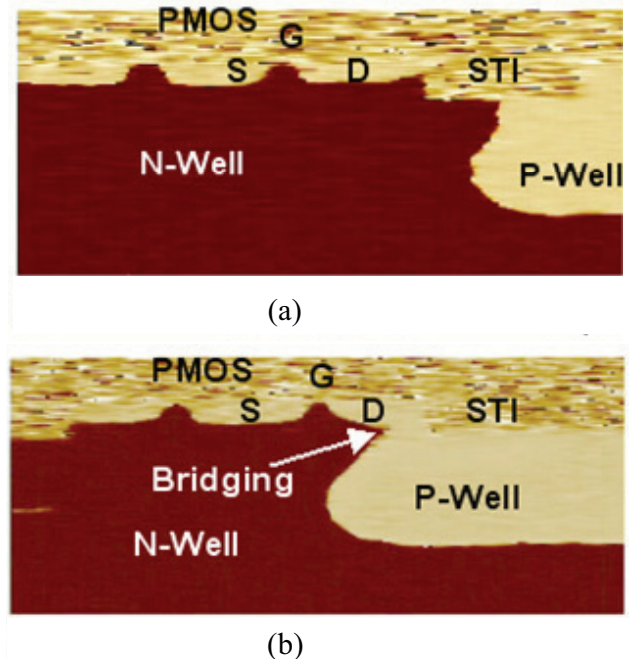


Figure 3: Cross-sectional SCM  $dC/dV$  phase images showing (a) the drain region is isolated by STI from the region of the P-Well in the normal device, (b) the drain region bridges the region of the P-Well in the failed device.

Since the implantation of the P-Well was performed on other devices at the same time during the manufacturing process, it might also cause the failure of those particular devices. This physical result gives a clue to check the regions of the output driver transistor circuits that adopt the P-Well implantation. Thus, one of the DQ pads that failed due to a high output leakage current,  $I_{LOH}$ , during the DC test was selected for further analysis. Figure 4 confirms the DQ pad failed in our FIB nanoprobeing tests when applying voltages to the  $V_{DD}$ ,  $V_{SS}$ , and DQ pads, respectively. The failed DQ pad indicates a very high output leakage current that is outside the production specification.

This DQ pad was then de-processed to the layer of M0 BL (bit line). A schematic layout of this pad and its adjacent circuitry is shown in Fig. 5. The power from  $V_{DD}$  will go to the PMOS transistor and the N-Well, and the power from  $V_{SS}$  will go to the NMOS transistor and the P-Well. The DQ voltage will go to the PMOS and NMOS transistors. The white dots surrounding the PMOS indicate the contacts to the N-Well, and those surrounding the NMOS indicate the contacts to the P-Well.

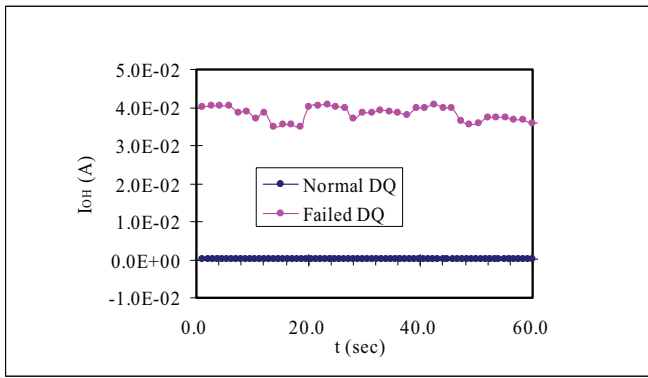


Figure 4: Output leakage currents of the normal and failed DQ pads.

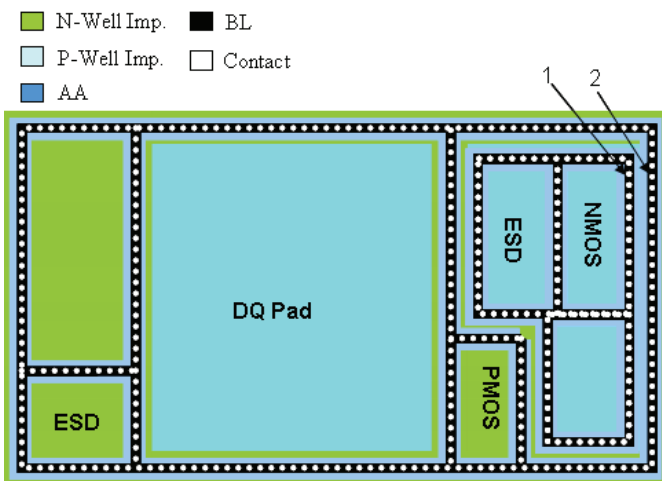


Figure 5: A schematic layout showing the areas of the DQ pad and its adjacent circuitry.

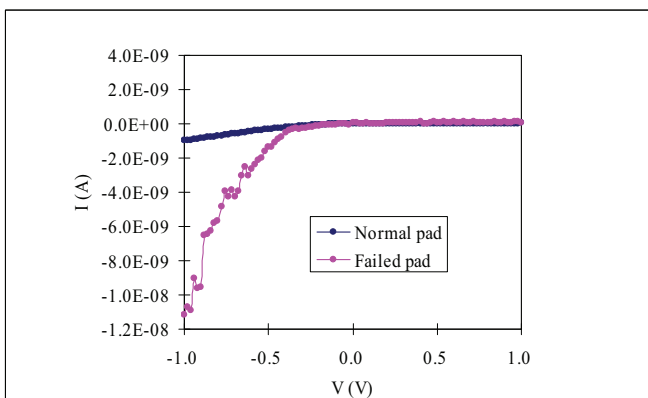
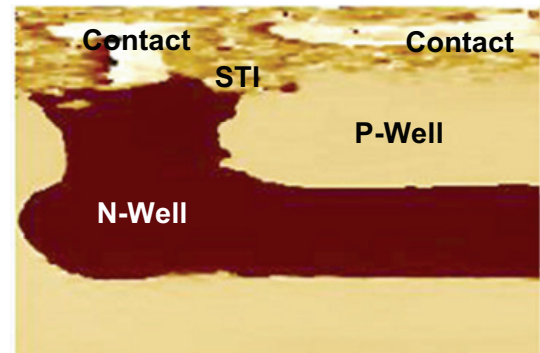
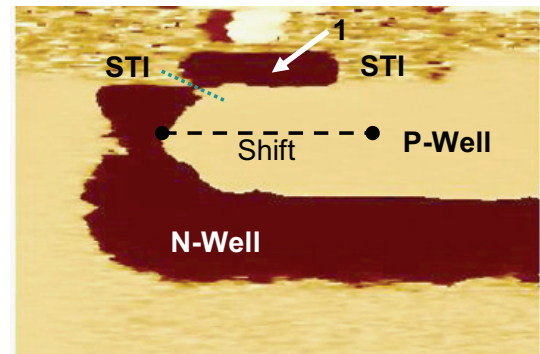


Figure 6: Current-Voltage characteristics of a P-N junction diode in the normal and failed DQ pads.



(a)



(b)

Figure 7: SCM  $dC/dV$  phase images showing the profiles of the P-Well and N-Well in (a) the normal and (b) the failed devices.

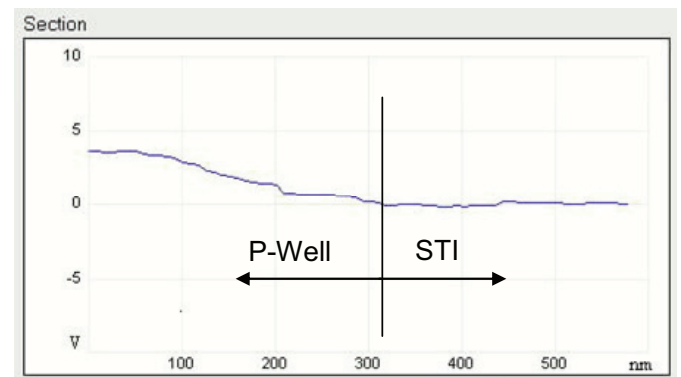


Figure 8: A section analysis of SCM signals along the dashed green line of Fig. 7b.

Since the  $I_{LOH}$  failed in the DC test, the NMOS circuit was therefore investigated. In addition, a P-Well shift was observed earlier in the failed low  $V_t$  PMOS of the SA circuit, so we simply probed two Well contacts (one P-Well and one N-Well) as indicated by arrows 1 and 2 in Fig. 5 at the NMOS to examine the I-V characteristics. Figure 6 shows the I-V curves in the normal and failed DQ pads. Both curves behave as a P-N junction diode. Nevertheless, the current in the failed pad is higher than in the normal pad at the same forward-biased condition.

From the cross-sectional SCM phase images along the two Well contacts, it can be seen that the P-Well has shifted to the left side of the normal position that separates the original N-Well into two regions (Fig. 7a and 7b). In addition, a sectional analysis of SCM data (Fig. 8) along the dashed green line in Fig. 7b confirms the N-Well has been separated into two regions by the shift of the P-Well even in the area between STI and the P-Well. Therefore, as indicated by arrow 1 (Fig. 7b), the areas of the P-N junction and the N-Well in the failed pad are smaller than those of the normal pad. This probably causes a higher current at the same forward-biased condition because the area of the depletion region of the P-N junction is reduced compared to that of the normal pad.

From the results mentioned above, we conclude that the shift of the P-Well during the manufacturing process causes the failure of a high output leakage current in the DC test for this specific case.

## Conclusions

In this paper, the failure analysis process for a specific case that is failed due to a high output leakage current in the DC test is demonstrated. Nanoprobing is a useful tool for the confirmation of electrical characterization and localization of device failures. Moreover, SCM provides helpful 2-D implantation doping profiles for the verification of physical causes of the failure devices. In this specific case, the shift of the P-Well during the manufacturing process is identified as the cause of DC failure.

## Acknowledgments

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## References

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