

MAXIMUM PERMISSIBLE EB ACCELERATION VOLTAGE FOR SEM-BASED INSPECTION BEFORE ELECTRICAL CHARACTERIZATION OF ADVANCED MOS

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ABSTRACT

The electron beam based inspection instruments such as the Review-SEM are widely used to analyze defects during manufacturing and failure analysis of scaled devices. Nano-probers used for scaled devices analysis also employs SEM for probe guidance. However, electron beam (EB) induced damages are increasing with the scaling. A higher SEM resolution induces device damage. To avoid the damage, the acceleration voltage should be lower. Several generations of scaled devices from 350nm to 65nm were examined, and critical EB acceleration voltage that induced device degradation was quantitatively evaluated. The determination mechanism of permissible electron beam acceleration voltage is clarified.

INTRODUCTION

Electron beam based inspection methods such as CD-SEM (Critical Dimension SEM), and Review-SEM have become indispensable in the manufacturing and development area [1]. Also, the Nano-prober with SEM guidance has become important in the failure analysis area to evaluate the localized device in the actual LSI [2]. However, these instruments should be used without inducing gate oxide damages by EB, which is known to induce device degradation [3-4]. For scaled devices, permissible acceleration voltage and its relation to the device structure have not been reported. A higher SEM resolution induces device damage. To avoid the damage, the acceleration voltage should be lower. In the present work, we prepared scaled devices with generations from 350nm to 65nm, and evaluated device degradation for several acceleration voltages. Indeed, the maximum possible accelerating voltage reduces with smaller device technologies. The determination mechanism of the voltage is discussed.

EXPERIMENTAL

In this work, we evaluated Pass-MOS (thin gate oxide NMOS) in SRAM cells with the SEM based Nano-Probing System [2], where the tungsten plugs of 100nm in diameter are probed by tips of 90 nm apex with the guidance of the SEM image. In order to probe the individual FET, the wiring layers of the target devices were mechanically polished to expose isolated tungsten plugs to the source, drain and the gate (Fig. 1). The Nano-probing is performed using 1kV guidance SEM. This condition was confirmed beforehand to be safe, and the characteristics change of V_{th} , I_{ds} and S -values were within 0.5% difference, by comparing Test Element group (TEG) based data (without electron irradiation) and Nano-Probing data (after electron irradiation) on the same devices. First, the "initial" I_{ds} - V_{gs} characteristics of the actual device are measured. Then, the SEM acceleration voltage was raised to a fixed condition between 1kV and 6kV, and the I_{ds} - V_{gs} characteristics were measured after electron beam irradiation of 60 seconds, with the gate, drain, source, and the substrate grounded. The exposure dose was on the order of 10^{-6}

C/cm^2 , calculated from channel size, electron beam scan area, and the current measured by a Faraday cup. V_{th} is the gate voltage at $I_{ds}=10nA$, I_{ds} is the current at $V_{ds}=V_{gs}=V_{dd}$, and S is the subthreshold slope between $10^{-8}A$ and $10^{-9}A$. ΔV_{th} , ΔI_{ds} and ΔS are the difference between prior to and after electron beam irradiation.

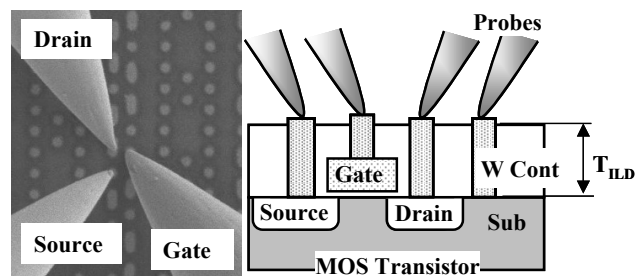


FIGURE 1. SEM photograph of Nano-Probes and schematic diagram of device cross-section during measurement. T_{ILD} shows layer thickness between Silicon and electron irradiation surface.

RESULT AND DISCUSSION

Figure 2 shows I_{ds} - V_{gs} curves of a 90nm generation device prior to and after electron beam irradiation at 5kV. V_{th} , I_{ds} , and S are found to degrade. The degradations were mainly caused by the increase of gate oxide interface states density. Fig. 3 shows, the electron beam acceleration voltage dependence of ΔV_{th} , ΔI_{ds} and ΔS . Device degradations of ΔV_{th} , ΔS , and ΔI_{ds} were confirmed to start at the electron beam acceleration over 4kV. Starting acceleration voltages of device degradations is defined as V_{crit} . Relationship between the V_{crit} and device generation between 350nm and 65nm is

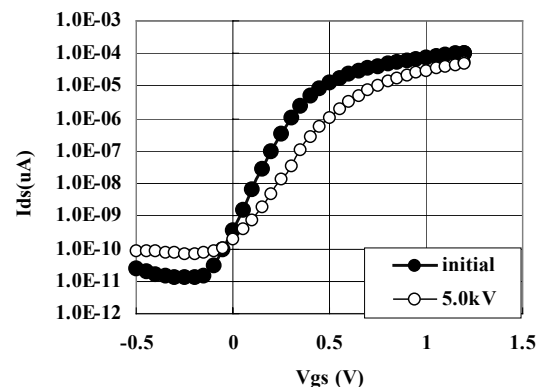


FIGURE 2. I_{ds} - V_{gs} characteristics of "initial" and after electron beam exposed at 5kV of a 90nm device. Solid circles show I_{ds} - V_{gs} of initial characteristics and open circles show after.

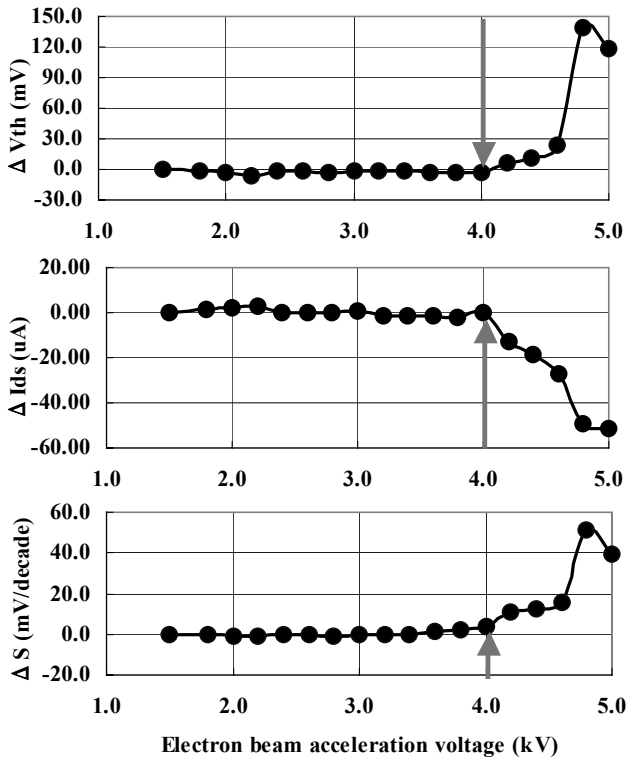


FIGURE 3. The electron beam acceleration voltage dependence of ΔV_{th} , ΔI_{ds} , and ΔS . The arrows show V_{crit} (starting voltage of device degradation).

shown in Fig. 4. The V_{crit} lowers with the device generation. Consequently, SEM observation should be performed with lower acceleration voltage on the scaled devices. The change of the V_{crit} is attributed to the vertical structure change of the device, mainly ILD (Inter Layer Dielectric) and gate electrode thickness. To confirm this, we polished the device to reduce the distance between the silicon surface and electron irradiation surface, which is defined as T_{ILD} (Fig 1). Using 90nm and 250nm devices, we evaluated the relationship between V_{crit} and T_{ILD} , as shown in Fig 5. V_{crit} - T_{ILD} relations are on the same curve even for the different generation devices. The maximum penetration depth of electron at each

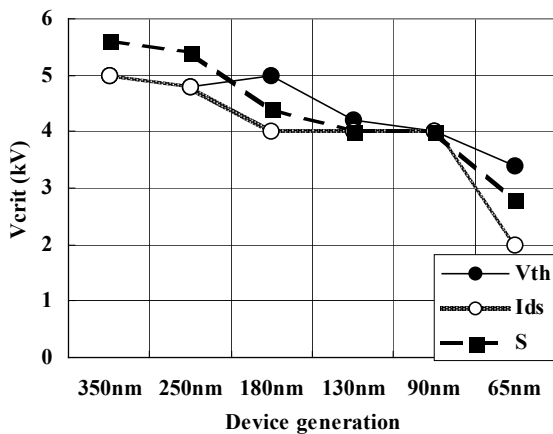


FIGURE 4. The V_{crit} (starting voltage of device degradation) vs. device generations. Solid circles show V_{th} , Open circles show I_{ds} , and solid squares show S .

acceleration voltage is calculated by the Monte Carlo simulation [5], and also plotted on the Fig 5. When the maximum penetration depth is plotted on the same axis as the T_{ILD} , V_{crit} and the voltage which is given by the simulation correspond well. This implies that the T_{ILD} and the maximum penetration depth are the same physical quantity. Therefore, the device degradation starts when the irradiated electron beam reaches the MOS gate insulator, T_{ILD} under the EB irradiation surface. The device degradation should be small for the electron irradiation with less than the V_{crit} .

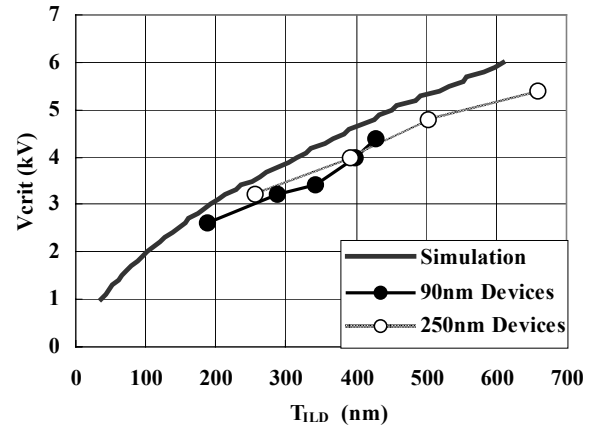


FIGURE 5. The V_{crit} (starting voltage of device degradation) vs. T_{ILD} (layer thickness between Silicon surface and electron beam irradiation surface). Solid circles show 90nm device and open circles show 250nm device. Solid line shows the maximum penetration length of electron that was calculated.

CONCLUSION

The influence of device characteristics by the electron beam irradiation during CD-SEM, Review-SEM, and Nano-Probe observation was studied. The maximum permissible electron beam acceleration voltage is determined the thickness between silicon surface and electron irradiation surface (T_{ILD}). With the scaling of the devices, the electron irradiation voltage must be tuned lower than the maximum voltage during device inspections in manufacturing control and in failure analysis procedure.

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