

Advanced electrical analysis of embedded memory cells using Atomic Force Probing

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Abstract

To identify the failure cause of embedded memory cells - e.g. SRAM with 6 transistors - it is often necessary to measure the electrical parameters of each transistor. Until now, on integrated circuits with small feature size and pitch, this was only possible using FIB probing pads or SEM probers, but both methods are complex and error-prone. Today Atomic Force Probing (AFP) provides a powerful alternative, allowing fast and non-destructive characterization of single transistors. In this paper the functional principle of the technique is introduced. Three case studies of SRAM, ROM and NVM cells illustrate the successful application of this nano-probing tool.

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1. Motivation

A failing cell in an embedded memory can usually be localized by ATE testing in combination with built-in self-test features (MBIST) of the device [2,3]. But when it comes to the identification of the failure cause, these tools have a blind spot regarding what is wrong inside of the cell. Some types of defects (e.g. large particles) can be found by cross-sectioning or delayering the die and analyzing the failing region by SEM imaging or voltage contrast. But if this approach is without success, further localization within the cell is required [1].

In case of such a challenging problem in an SRAM cell with 6 or more transistors it is necessary to measure the electrical parameters of each single transistor. Until a short time ago, on CMOS devices with feature sizes of 180nm and below this was only possible by using FIB probing pads (fig. 1) or SEM probers. But both methods have considerable drawbacks.

Disadvantages of FIB probing pads:

- The preparation effort is very high.
- On densely packed layouts the preparation is error-prone because the spacing is too narrow for reliable FIB contacting.
- There is a considerable risk of transistor parameter drift by implantation of Ga ions [4,5].
- The access to circuit nodes is quite limited. It is hardly possible to measure more than one transistor inside of a cell because the FIB probing pads cover the adjacent transistors.

Disadvantages of SEM probing:

- Due to the lack of a force control mechanism, sample and probe needle are exposed to high mechanical stress.
- Surface contamination by the electron beam might lead to contact problems.
- Contacting and measurement is error-prone on small geometries because the contact point of the probe tip is not visible in the e-beam image.

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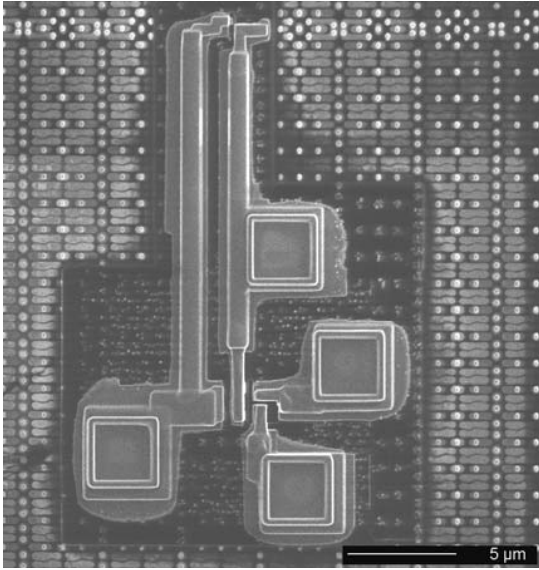


Fig. 1. FIB probing pads for measurement of one complete SRAM cell (single transistors can not be measured), access to adjacent cells is obstructed

Recent advancements of Atomic Force Probers (AFP) provide a powerful alternative avoiding these problems. This tool allows fast and accurate DC characterization of single transistors in an integrated circuit while keeping preparation side effects at a minimum.

2. Functional principle of AFP nanoprobing

The basic technique of atomic force nano-probing is quite similar to a conventional Atomic Force Microscope (AFM). Using piezo actuators and force feedback control, an AFP probe scans the region of interest on a sample to create a high resolution topographical map of the surface. This AFM image is subsequently used to position the same probe on a circuit node (e.g. a tungsten contact plug) to make a low-resistance ohmic connection (fig. 4). Then the DC characterization can be done using a parameter analyzer connected to the probes (fig. 5). The main differences to a conventional AFM are:

- Two or more probes are used simultaneously. The topographical images created by each probe can be aligned to each other (fig. 4).
- The probes can be positioned extremely close to each other. This can be achieved by using sharp tungsten needles instead of conventional AFM probe tips [6].

The best sample preparation method for single transistor measurement on an IC is the removal of all metal layers by mechanical polishing. Then the probes have direct access to all transistor terminals (fig. 2,3). For contrast enhancement of the AFM micrograph, a few nanometers of topography can be created by a slight oxide etch (fig. 4).

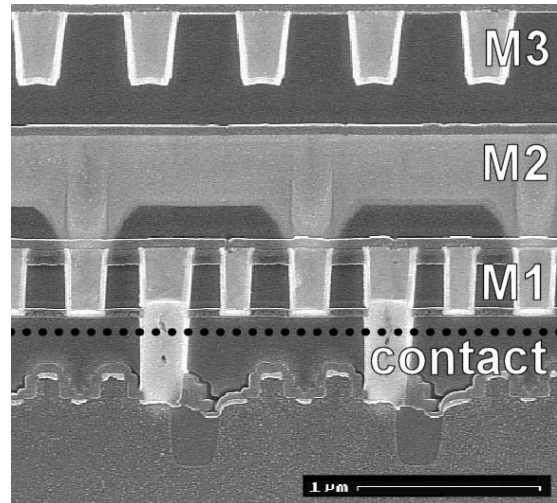


Fig. 2. Typical cross-section of an SRAM, dotted line indicates the preparation target

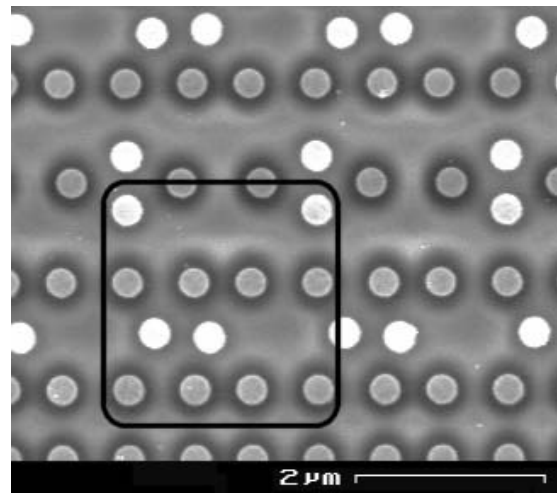


Fig. 3. SEM micrograph of a top-down polished sample (area of one SRAM cell marked by rectangle), contact plugs grant access to all transistor terminals

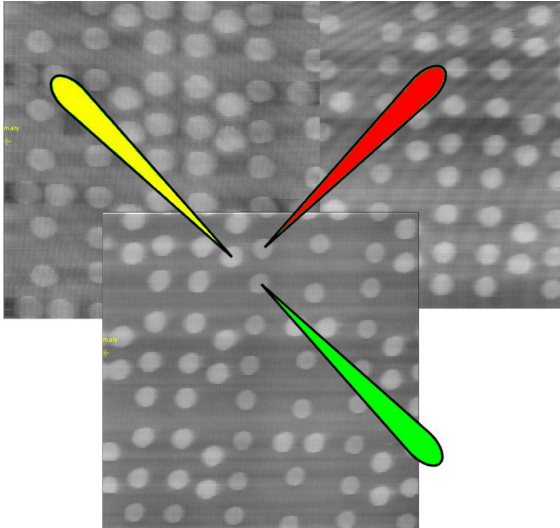


Fig. 4: Topographical AFM image of the polished SRAM sample (overlay of 3 probes) used for positioning the AFP probes on the tungsten contact plugs

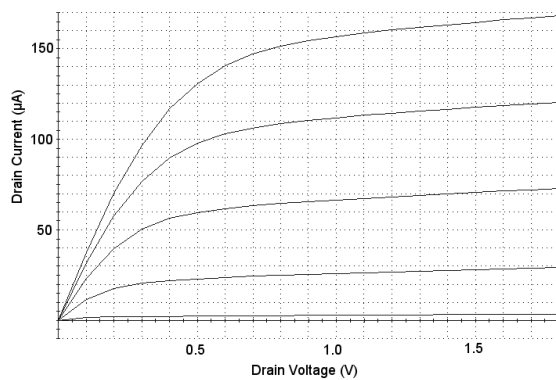


Fig. 5: Transistor parameters of a 180nm n-FET measured via 3 AFP probes on source, drain and gate

3. Case studies

The preparation and measurement techniques described above were successfully used in the following analysis cases.

3.1. SRAM single cell failure

This example shows a single cell failure of a standard 6T single port SRAM manufactured in a 180nm process. After polishing the sample down to contact level, all 6 transistors were characterized using AFP. First the diodes between the source/drain regions and n-well/substrate were measured. All diode curves were without objection. The second step was the acquisition of the ID-vs.-VD family of curves and the ID-vs.-VG curve of each transistor. While 3 n-FETs and 2 p-FETs were without objection, one n-FET showed a leakage current between source and drain (fig. 6). The subsequent TEM cross-section revealed a dislocation (silicon crystal defect) causing a leakage path through the channel region of this n-FET (fig. 7).

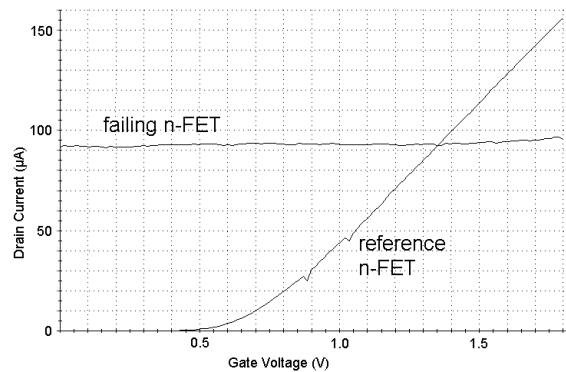


Fig. 6: ID-vs.-VG characteristic shows leakage between source and drain

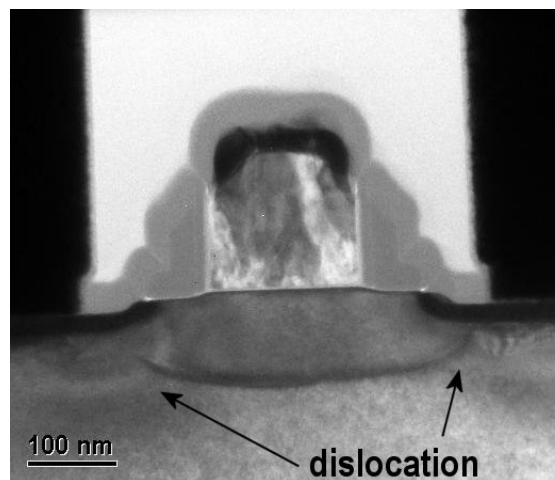


Fig. 7: TEM cross-section micrograph, dislocation causing leakage between source and drain

3.2. ROM bitline failure

The second example shows a 130nm diffusion-type ROM with a complete failure of one bitline (BL). Backside emission microscopy showed a spot within the cell array at the failing bitline, leading to the assumption that the BL fail was actually caused by a single defective cell. The bitline address of this cell was already known from the ATE test, but the optical resolution of the photo-emission spot was too poor to identify the exact wordline address. Therefore all possible candidates (approx. 10 BL contacts) were measured by AFP to localize the failing cell. Thus it was possible to identify one of the contacts having a leakage current to the n-well (fig. 8).

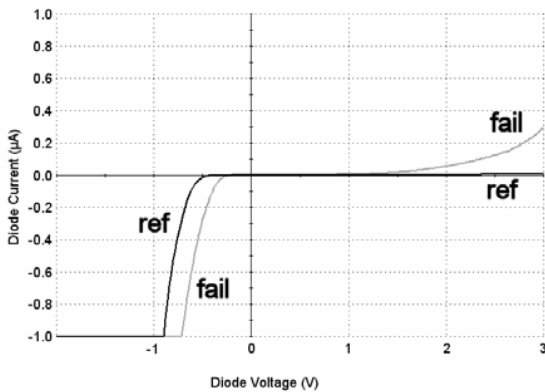


Fig. 8: Leaking bitline contact in comparison to a good reference contact

A TEM cross-section revealed a dislocation underneath the gate of the transistor connected to the leaking BL contact (fig. 9).

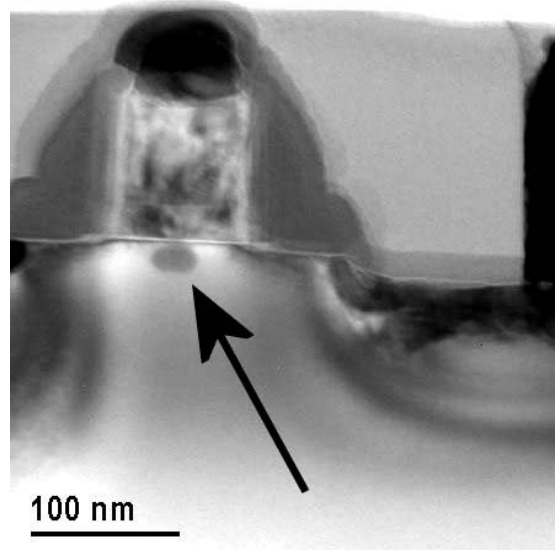


Fig. 9: Dislocation at one of the transistors connected to the leaking bitline contact

3.3. Direct read/write of an NVM cell

The subject of this example is not an actual failure but it illustrates the successful attempt to read and write a single cell of an embedded Non-Volatile Memory (NVM) in 0.25µm Flash technology.

The sample preparation was similar to the previously described examples. Using the tungsten contact plugs, the terminals of the NVM cell were connected to a parameter analyzer using the AFP probes. The logical state of the cell is reflected in the threshold voltage of the FET and can be determined by measuring the I_D -vs.- V_G characteristic. By applying a programming voltage pulse of +15V the threshold voltage could be shifted by approx. 5V (fig. 10). The cell could be erased by applying a negative programming voltage of -15V. These program and erase operations were repeated several times to prove that the effect was reversible and reproducible. Fig. 10 shows several curves compiled from consecutive program/erase cycles.

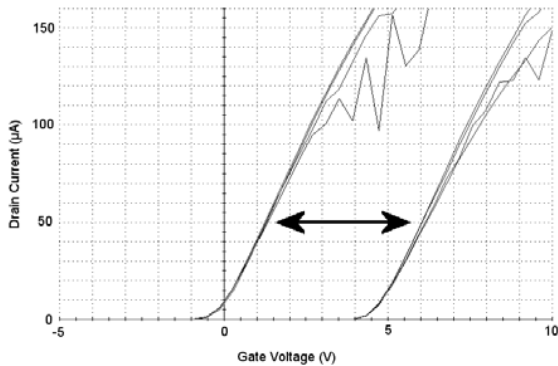


Fig. 10: Reversible shift of threshold voltage by applying +/-15V programming pulses via AFP probes

On most products with embedded NVM memories it is impossible to write single bits instead of whole data words or to vary the programming voltage. Therefore the direct access via AFP is a major step forward towards a precise characterization of the NVM cell parameters.

4. Conclusion

While in the past years commercial AFP systems have still suffered from mechanical instability, recently developed tools have advanced to a state where they can be used productively in a failure analysis lab.

The AFP technique has proven to be able to extend the range of failure localization by electrical characterization beyond the former geometrical limits. Besides the analysis of physical defects there are also other interesting fields of application. Resulting from ever shrinking feature sizes and decreasing supply voltages, experts predict that statistical parametric deviations and local mismatches of aggressively designed memory cells will play a larger role as yield detractors. Due to the non-invasiveness of the preparation, AFP-assisted DC characterization is a suitable way to verify device libraries of a certain technology node by comparing the measured transistor parameters to simulation data.

Therefore there will be a significantly higher demand for single transistor characterization for forthcoming technology generations. The AFP method looks like a very promising candidate for covering these needs.

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