Proceedings of the 32nd International Symposium for Testing and Failure Analysis
November 12-16, 2006, Renaissance Austin Hotel, Austin, Texas, USA

Development of Backside Scanning Capacitance Microscopy Technique for Advanced SOI Microprocessors

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Abstract

Implant related issues are hard to detect with conventional techniques for advanced devices manufactured with deep sub-micron technology. This has led to introduction of site-specific analysis techniques. This paper presents the scanning capacitance microscopy (SCM) technique developed from backside of SOI devices for packaged products. The challenge from backside method includes sample preparation methodology to obtain a thin oxide layer of high quality, SCM parameters optimization and data interpretation. Optimization of plasma etching of buried oxide followed by a new method of growing thin oxide using UV/ozone is also presented. This oxidation method overcomes the limitations imposed due to packaged unit not being able to heat to high temperature for growing thermal oxide. Backside SCM successfully profiled both the n and p type dopants in both cache and core transistors.

1. Introduction

As the silicon process technology scales to deep sub-micron regime, it has become a great challenge to physically identify the implantation related issues in the failure analysis flow. The lower resolution techniques such as Spreading Resistance Profiling (SRP) and Secondary Ion Mass Spectrometry (SIMS) are not site-specific as required for failure analysis. Chemical staining has also been used but is difficult to control. This leads to inconsistency and an inability to reveal both n & p type of dopants simultaneously [1]. Moreover, the threshold for chemical staining is rather high for dopant concentration at $1x10^{17}$ atoms/cm^3. Scanning probe microscopy based techniques such as Scanning capacitance microscopy (SCM) and Scanning Spreading Resistance Microscopy (SSRM) offer a capability for dopant profiling with nanometer scale lateral spatial resolution [2].

SCM is a powerful technique with ability to image the dopant profile in both planar and 2-dimensional views with added advantage that distinction between n and p-type dopants is feasible as compared to SSRM. A Scanning Capacitance Microscope is an atomic force microscope (AFM) equipped with a high sensitivity capacitance sensor. The SCM provides the spatial resolution of about 15-20nm and has a dynamic range of $1x10^{15}$ – $1x10^{20}$ atoms/cm^3 [2].

2. SCM Working Principle

In SCM, the metallized probe forms a metal-insulator-semiconductor (MIS) capacitor with the semiconductor sample as shown schematically in Fig 1 [3]. An AC bias applied between the scanning contact tip and the sample generates capacitance variations, which are monitored using a GHz resonant capacitance sensor. The system is capable of sensing variations smaller than attofarads ($<1x10^{-18}$ F). The capacitance variation (dC/dV) is a measure for the local carrier concentration density and the type of dopants (i.e. n or p) dopants. The capacitance changes with applied ac voltage as there's accumulation and depletion leading to capacitance variation as shown schematically in Fig 2. Different type of dopants results in a different sign of the dC/dV signal. Moreover different dopant level results in a different intensity of the dC/dV signal and thus SCM analysis can be used for high resolution dopant profiling.

The AFM mode simultaneously gives topography information hence both topography and SCM data enables the direct correlation of a feature location with its dopant imaging. This ability gives a valuable data for failure analysis. It allows analysis at the suspected fail location whether a particular implant is present and has the right type of dopants and the expected dimensions. In most of the cases, a comparison is done with a passing location to identify differences. SCM usefulness lies in the fact that it has the ability to analyze site-specific fail location to the transistor level with the required spatial resolution and implant concentration sensitivity.

In literature, most of the work is reported on planar SCM using the frontside approach [4]. However it suffers from difficulty in etching the cobalt silicide layer present on the active area. Moreover, due to the presence of buried oxide (BOX) insulator layer in SOI devices, the conductive path required to bias the sample is unable to be formed during SCM scanning. This makes the conventional planar SCM imaging not feasible on silicon-on-insulator (SOI) devices. Another commonly used method is cross-section polishing method, which is unsuitable for site-specific analysis.

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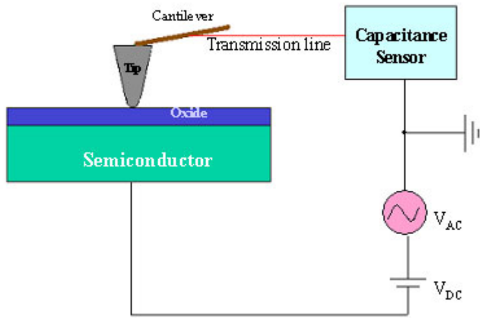
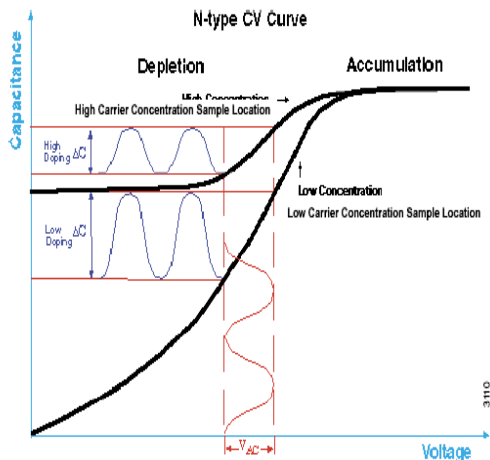


Fig 1. Schematic Set-Up of Scanning Capacitance Microscopy Technique.



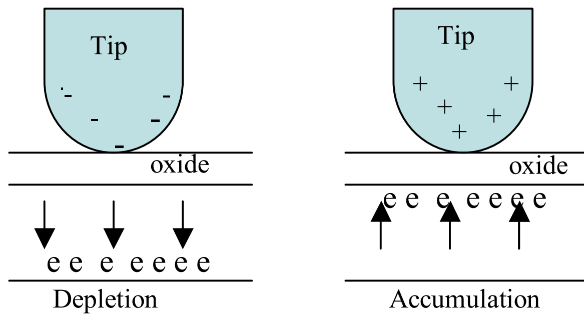


Fig 2. A typical CV curve for NMOS transistor and a schematic showing depletion and accumulation. SCM measures dC/dV signal with low carrier concentration giving deeper depletion and hence have higher capacitance change (ΔC) while high carrier concentration has a shallower depletion leading to lower ΔC.

In present work that is being reported for the first time, planar SCM technique has been developed from backside for AMD's advanced Silicon-on-Insulator (SOI) microprocessors based on 90nm process technology node. Backside SCM is a site-specific method with the ability to navigate to specific fail location. It is applicable to a flip-chip packaged die without the need to remove the die from package. It could easily overcome the limitations exerted by insulating BOX layer as BOX layer is etched away and a conductive path is formed from metal interconnects and through the C4 bumps to package pins. Additionally, most of the semiconductor layers are still intact enabling further failure analysis if it is needed.

3. Experimental Details

The initial part of the work involved formulating a sample preparation technique for backside planar SCM imaging for SOI devices. The later part of the work evaluated the feasibility of backside SCM scanning of the SOI devices.

The packaged unit is deprocessed from backside to buried oxide (BOX) layer using precision polishing to polish down to a thickness of less than 150um. This is followed by silicon etch based on Tetra Methyl Ammonium Hydroxide (TMAH) etch chemistry [5]. TMAH etches silicon with high selectivity against silicon oxide and after etching silicon it essentially stops at the BOX layer. The BOX layer is then removed using plasma etch tool. A carbon tetra-fluoride (CF_4), trifluoromethane (CHF_3) and oxygen based plasma chemistry is used with low pressure and medium power for an optimized amount of time. The gas chemistry ensures that the active area is not attacked during the BOX plasma etch. This is followed by treating the unit with dilute hydrofluoric acid (HF) to remove the native oxide and expose silicon active area surface for subsequent controlled oxidation. The oxidation step is immediately carried out to prevent native oxide from forming.

The widely used method of growing thin high quality oxide using thermal baking at 250^0C couldn't be used for packaged unit. This is due to the fact that the solder bumps/under-fill would melt/deform for the packaged unit causing thinned die to crack. Therefore, a low temperature oxidation method was required for packaged unit. Two different approaches utilizing UV/ozone assisted oxidation and wet oxidation were evaluated. For UV/ozone oxidation method, a commercially available UV/ozone photo cleaner that combines UV light of wavelength 254 nm and 185 nm was used. Sample was exposed under UV/ozone environment at room temperature. Another method based on wet oxidation utilizing hydrogen peroxide (H_2O_2) was also evaluated.

DI 3100 AFM tool with SCM module was used for present work. A commercially available PtIr tip with 15 nm tip radius with a force constant of 2 N/m was used in contact mode. AC bias ranging between 1 to 2 V was applied while maintaining DC bias at 0 V. The analysis was carried out at ambient conditions.

4. Results & Discussion

Optimization of sample preparation methodology mainly involved BOX plasma etching and oxidation strategy. The backside deprocessing involving TMAH etch has already been established [1]. The BOX plasma etch time is found to be critical. A slightly higher etch time will result in over-etching causing silicon active area to be attacked. While lower etch time causes no dopant signal as BOX remaining is too thick as shown in Figs 3 & 4. In both the cases, UV/oxidation is carried out after plasma etching of BOX layer. Based on AFM topography and SCM data, the optimized plasma etch time was obtained.

Moreover, a thin layer of BOX is retained with this time so as not to cause native oxidation of silicon active area leading to dopant loss.

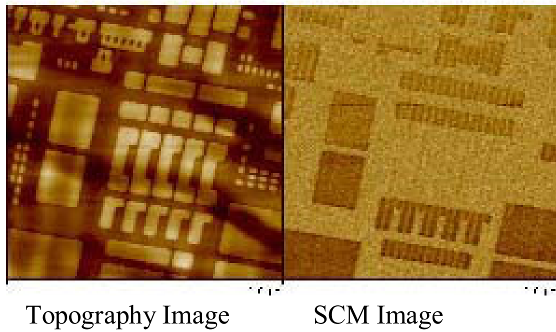


Fig 3. BOX plasma etching using higher etch time. Topography image showing that over-etch has occurred as active area (white color) 'stands out' in topography image.

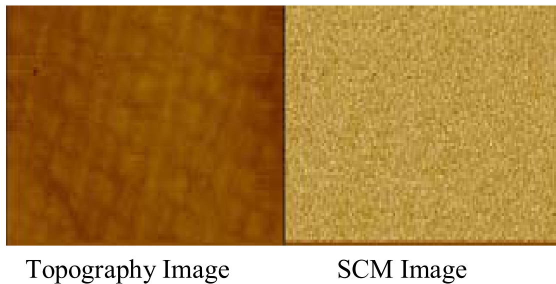


Fig 4. BOX plasma etching in under-etch conditions. A thick oxide is still remaining leading to no SCM signal

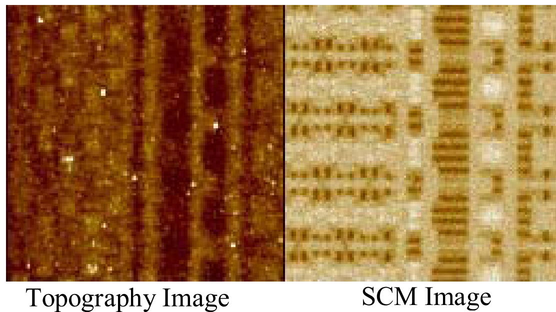


Fig 5. Sample after BOX plasma etch only i.e. without any oxidation.

SCM analysis of the sample without growing any oxide i.e. after the plasma etching of BOX provided low signal intensity as shown in Fig5. This indicated that oxidation to obtain a high quality oxide layer is critical for SCM analysis. Wet oxidation, which involves exposing unit in H_2O_2 solution, produces an oxide that gives reasonable SCM signal as shown in Fig 6. However, the SCM image contrast is not as distinct as UV/ozone method. Wet oxidation in general will introduce more contamination and rougher surface as compared to UV/ozone method leading to inferior signals. UV/ozone method with optimized etch time was found to produce good quality oxide as shown in SCM images in Fig 7. It is believed that ozone initially absorb on the silicon surface and then atomic oxygen is formed by dissociated UV radiation resulting in silicon oxide formation. [6]. This method does not involve heating the unit as the oxidation is carried out at room temperature, thus unit at package level can be imaged directly. The across die uniformity is found be dependent on plasma etching. It is an important factor for obtaining a good SCM image in both center and edge of die, which was confirmed by TEM cross-sectional analysis. A plasma chamber clean step using oxygen chemistry before etching the unit was found to give consistent results.

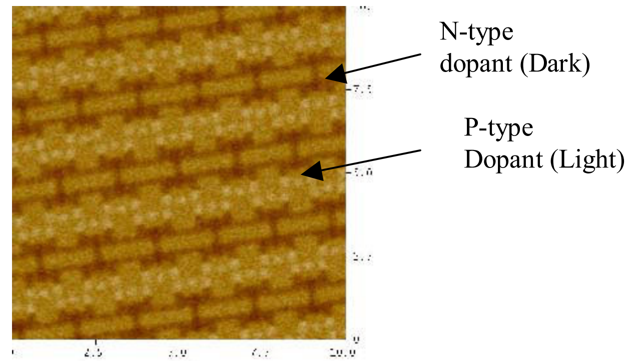


Fig 6. Sample after Hydrogen Per-oxide wet oxidation showing inferior resolution. SCM image appears to be low in signal.

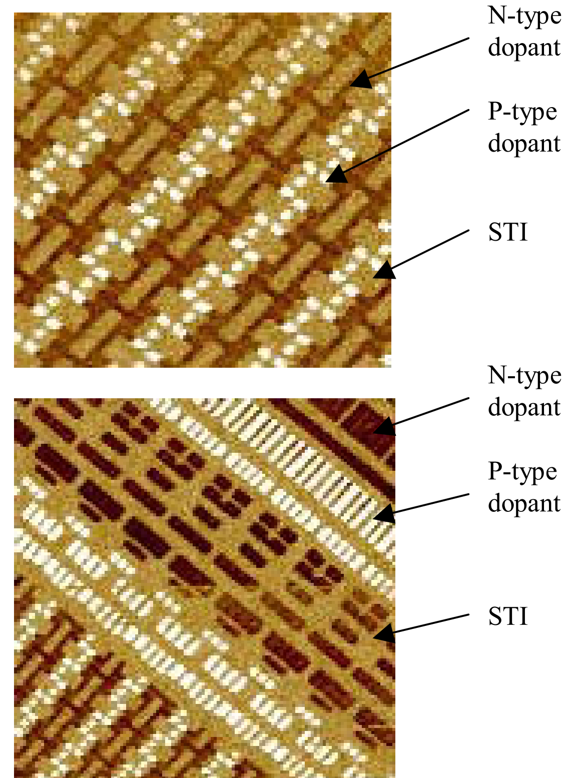


Fig 7: Sample after UV/Ozone Oxidation for 20 minutes at room temperature. Both cache with dense memory array (top) and control logic circuit (bottom) show good resolution image with distinct contrast between n and p type of dopant.

Backside dopant profiles for both n and p type of dopants were obtained with excellent contrast and good resolution with the optimized UV/ozone oxidation method. Both cache having dense memory array and core with isolated transistors showed well-defined dopant profiles. Good correlation of n and p doped active area critical dimensions (CD) as compared to Knights CAD layout measured CD was observed. This gives an ability to do some general quantitative measurements.

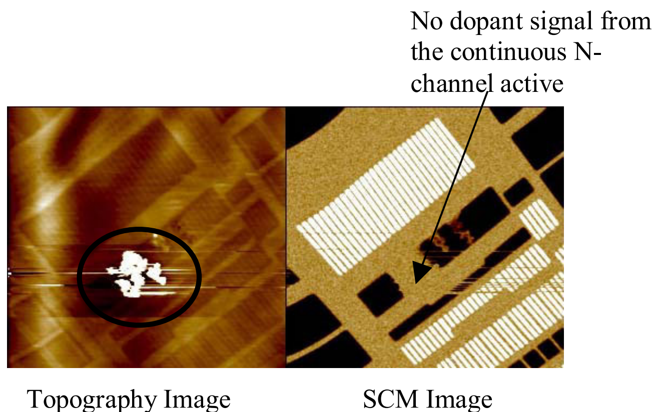


Fig 8. SCM analysis results for boundary scan failure at I/O pads. Dopant contrast appeared to be same near to the fail site as compared to nearby good site, indicating that the temperature involved in silicon active area damage was highly localized.

A unit failing JTAG boundary scan failure was subjected to SCM analysis. Fault isolation done using thermal induced voltage alteration (TIVA) technique showed presence of TIVA spots at the failing input/output pads. The unit was backside deprocessed to BOX level and optical microscopy showed a whitish spot at failing site. SCM analysis was performed for n and p type dopant profiling at the fail site. Plasma etching of BOX layer followed by UV/ozone oxidation was performed. AFM imaging showed some particle/debris at the fail location with no dopant signal at the failing spot as shown in Fig 8. Dopant contrast in the vicinity of the fail site appeared to be same as compared to nearby good site. It is suspected that the temperature involved at the damage silicon active area was highly localized and there was no dopant migration involved. Subsequent scanning electron microscope (SEM) inspection showed melted active area so no SCM signal was obtained at the fail area.

The backside SCM applications include uncovering implant related issues such as mis-aligned implants, incorrect implanted species and dosage, unexpected dimensions of implant species, source/drain diffusion shorts and narrowing down the wafer fabrication process step introducing the defect (at poly/spacer levels) by checking if implant is present/missing below the defect. This information is critical to determine the root cause of failures. If there are no implant issues observed, further physical failure analysis can be carried out from die backside, as all the layers are still intact.

5. Conclusions

In conclusion, a successful technique for dopant profiling for both n and p type of dopants using scanning capacitance microscopy has been developed. It is developed for packaged SOI devices from die backside and applicable for failure analysis applications. A new method of growing a high quality of oxide using UV/ozone oxidation has been developed. The backside SCM analysis is able to overcome the limitation of lack of substrate conductivity of front-side analysis for SOI devices.

Acknowledgements

The authors would like to greatly acknowledge the contribution from following people. Teo Chea Wei, Lutfie from DA lab and Edwin Goh, Ashok Anand and YC Mui from Advanced Packaging, AMD Singapore for helping in SCM analysis work. Jasmine Kam and Dr Du Anyan from IME, Singapore for helping in FIB/TEM work.

References

1. Lau YM, et al, "The Application of Scanning Capacitance Microscopy in Device Failure Analysis", *Proc. of 11th International Physical Failure Analysis Conf.,* 2004, pp99-102.
2. Wolf PD, et al, "Electrical characterization of semiconductor materials and devices using scanning probe microscopy", *Materials Science in Semiconductor Processing*, Vol.4, 2001, pp71-76.
3. Williams CC, "Two-Dimensional Dopant Profiling by Scanning Capacitance Microscopy", *Annual Rev. Mater. Sci.*, No.29, 1999, pp471-504.
4. "Electrical Characterization with Scanning Probe Microscopes", Veeco Application Note, http://www.veeco.com/appnotes/AN79_ElecChar_RevA0.pdf
5. Prejean S, Bruce V, Bruke J, " CMOS Backside Deprocessing with TMAH/IPA as a Sample Preparation Technique for Failure Analysis*", Proceedings from 28th International Symposium for Testing and Failure Analysis*, 2002, pp 317-323.
6. Tsuji O, Tatsuta T, Ogawa M, "Study of the Surface Oxidation using Silent Discharge Ozone combined with UV Irradiation", *Proceedings from 8th International Symposium on Plasma Chemistry*, 1987, pp1715-1719.