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Case Studies in Atomic Force Probe Analysis

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Introduction

The use of Atomic Force Probe (AFP) analysis in the analysis of semiconductor devices is expanding from its initial purpose of solely characterizing CMOS transistors at the contact level with a parametric analyzer. Other uses found for the AFP include the full electrical characterization of failing SRAM bit cells, current contrast imaging of SOI transistors, the probing of metallization layers to measure leakages, and use with other tools, such as light emission, to quickly localize and identify defects in logic circuits. The purpose of this paper is to present several case studies in regards to these activities and their results.

Case Study I: AFP SRAM Bit Cell Electrical Characterization

High Density SRAM Technologies (>100nm)
SRAM bit cell electrical characterization has proven to be a useful failure analysis tool in identifying the defects that cause single bit cell failures [1]. By analyzing the entire bit cell, the location and type of defect can be determined to help increase the probability of identifying the failure mechanism when the physical analysis is performed whether itís in the metal layers of the bit cell or in the transistors. This type of analysis is performed by depositing tungsten FIB pads on the bit line (BL), bit line bar (BLB), word line (WL), Power (VDD), and ground (VSS) (Figure 1) [2]. Micro-probe needles connected to a parametric analyzer are used to sweep BL and BLB; and to bias the WL, VDD, and VSS. Electrical signatures produced by the sweeping of the bit lines on a failing bit when compared to a passing bit cell usually indicates the type of defect causing the bit failure and its location within the bit cell.

AFP can be used in place of the traditional method using Focused Ion Beam (FIB) deposited tungsten/platinum pads and micro-probe needles (T-4-10). Figure 2 shows a 0.25um SRAM array that has been deprocessed to the top of Via 2. The bit lines at Metal 3 have been polished off to isolate the failing bit from the other bits in the array and to allow for the AFP to probe the bit line vias and the VDD and VSS vias. Because the AFP has only four available heads for probing, both the WL and VDD have to be powered with the same probe tip.

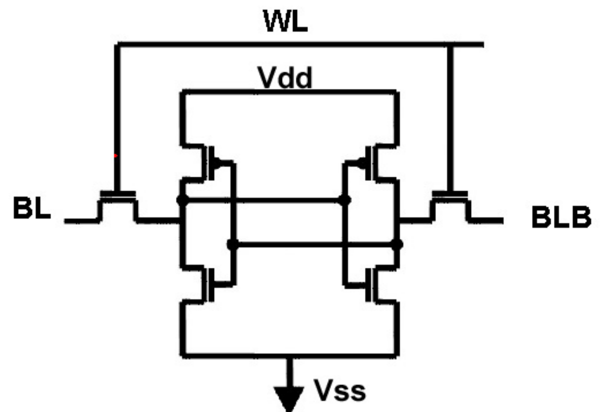

Figure 1: *Schematic of a 6T SRAM bit cell shows that five nodes BL, BLB, WL, VDD, and VSS have to be biased for the electrical characterization of the bit cell.*

The WL and VDD connections for the bit cell run the length of the array along the rows at Metal 2 layer for this technology. At the edge of the SRAM array the FIB is used to cut a small whole through the inter-level dielectric to expose the WL at Metal 2 (Figure 3). Tungsten is then deposited to make contact from the Metal 2 WL to VDD at Via 2 (Figure 4). Both the WL and VDD can be powered by one of the AFP tips at the VDD via at the failing bit location.

With this single FIB edit, the AFP can now be used to probe the BL, BLB, VDD/WL and VSS vias and analyze the failing bit cell (Figure 5). Figure 6 shows the electrical results for the failing bit cell. The electrical signature indicates that there was a resistive defect in path between the BL storage node and the BL contact to the bit line. Transmission Electron Microscopy (TEM) cross section analysis through the BL storage node and BL contact identified a poly-silicon defect in the BL pass gate transistor. This extra poly caused an increase in the length of the transistor channel increasing resistance. The physical analysis results matched the electrical analysis results produced by the AFP.

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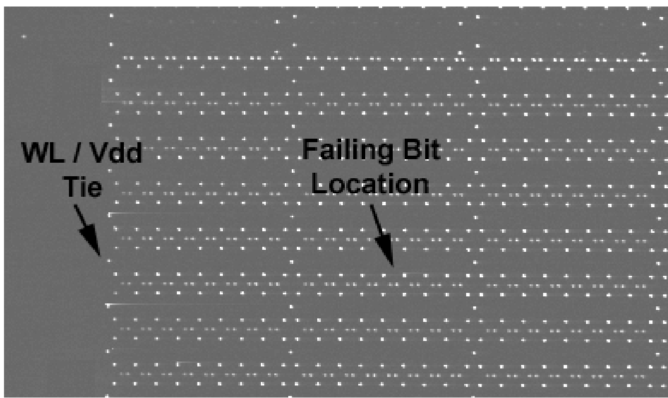

Figure 2: *Ion beam image of a 0.25 CMOS SRAM array. The Metal 3 bit lines have been polished off exposing the Via 2 plugs. The failing bit cell location and the location of the WL/VDD FIB connection at the edge of the array are shown.*

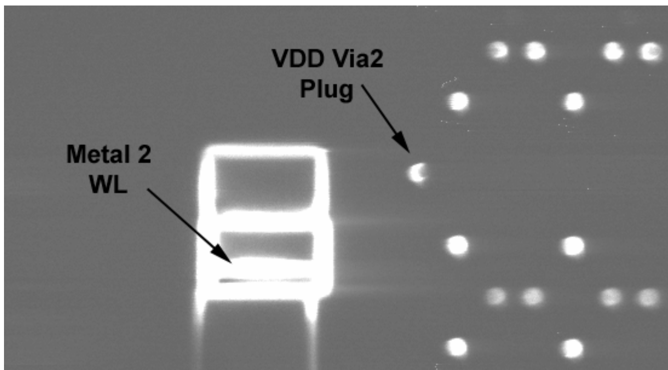

Figure 3: *Close-up ion beam image of at the edge of the array. A FIB hole was cut through the oxide to expose the Metal 2 word line.*

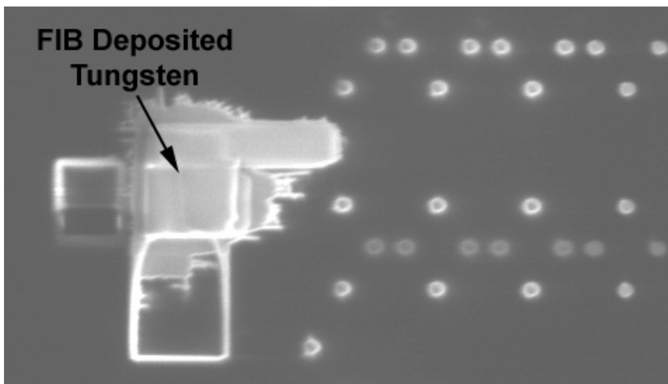

Figure 4: *Ion beam image at the edge of the array showing how tungsten is deposited to attach the word line to the VDD Via 2 plug.*

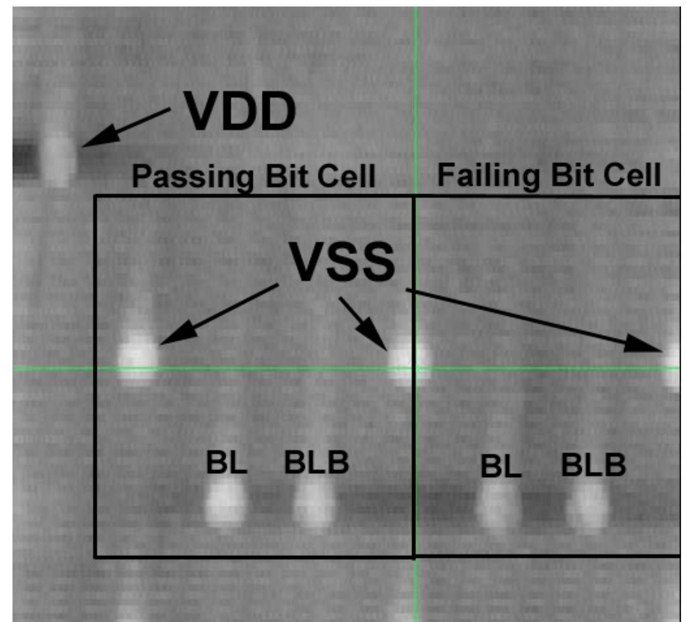

Figure 5: *Topographical AFP image of the top of Via2 plugs after the removal of Metal 3 for a failing 0.25um SRAM bit cell. A FIB was used to connect the word line (WL) to the VDD metallization. Complete bit cell characterization was performed with the AFP at these Via2 plugs.*

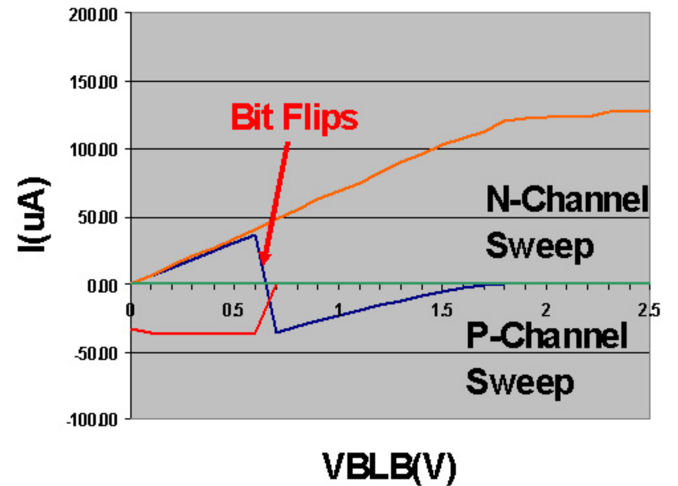

Figure 6: *AFP electrical characterization results for the failing SRAM bit cell. The bit cell flips data states when the bit line bar (BLB) p-channel load transistor is swept indicating a series resistance problem between the bit line (BL) storage node and the bit line connection to the bit cell based on Spice simulation models.*

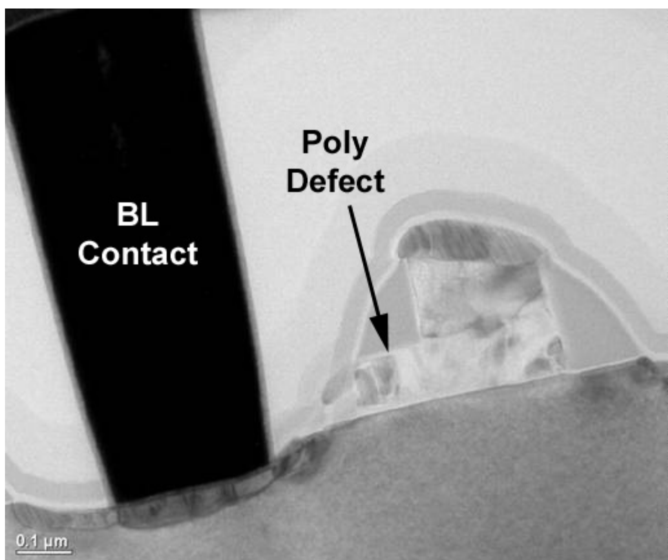

Figure 7: *TEM cross section image of the failing node shows a poly defect in the gate of the pass gate transistor. The length of the transistor channel is increased causing greater channel resistance just as the electrical analysis and Spice modeling had predicted.*

Ultra High Density SRAM Technologies (<100nm)

Full electrical characterization of sub-100nm high density layout SRAM arrays is more difficult, but can also be performed with the AFP. The type of AFP analysis described in the previous section, performed on the 0.25um SRAM bit cell, can not be performed on this SRAM layout due to the fact that probing at any of the vias at the bit cell level would require more than four probe heads to bias all the nodes. The layout does not allow for FIB edits to be made to reduce the overall number of nodes. Therefore a second approach had to be taken.

The entire bit cell circuit in the ultra high density layout is contained at Metal 1 and lower. Any defect at Via 1 or higher would produce a double bit failure at a minimum. Therefore, all the layers above Metal 1 can be ignored as the source of the failure in the analysis of single bit failures. Figure 8 shows a SEM image of a failing sub-100nm ultra high density layout SRAM bit cell. The sample was deprocessed to the top of Metal 1 with Via 1 still remaining. Inspection with a SEM did not reveal a short at the top of Metal 1 within the bit cell, eliminating that as a possible cause of the failure. However, metal shorts at the bottom of the Metal 1 layer or a resistive interface between one of the Metal 1 lines and its underlying contact would not be visible with SEM inspection. To eliminate these two failure mechanisms as a possible cause of the failure, the sample was polished to remove Via 1 and to planarize the very top of Metal 1 to the surrounding oxide so that AFP analysis could be performed. Figure 9 is the SEM image of the failing bit cell after the polish.

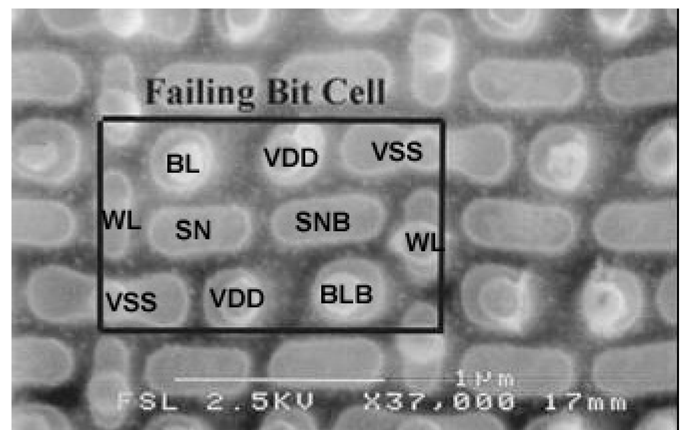

Figure 8: *SEM image of a failing 90nm ultra high density SRAM bit cell failure. The sample has been deprocessed to Metal 1 exposing Via 1 and Metal 1. SEM inspection did not reveal a short or defect at the top of Metal 1. (SN = storage node and SNB = storage node bar)*

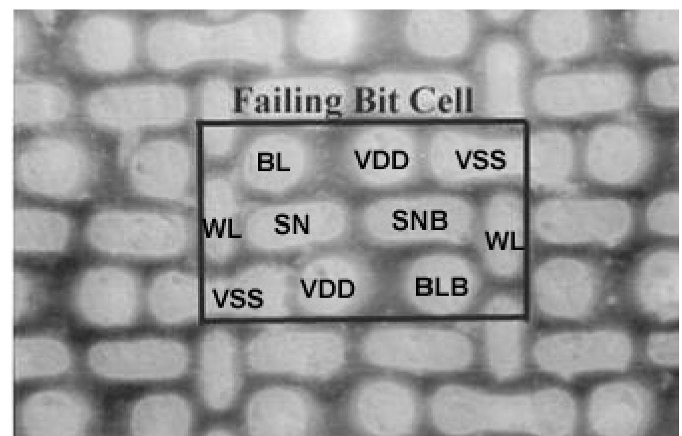

Figure 9: *SEM of Metal 1 after polishing to remove Via 1 and to planarize Metal1and the ILD0 for AFP analysis. The AFP is now able to scan and probe the Metal 1 to determine if the contact to Metal 1 interface is resistive or if there are metal shorts at the bottom of Metal 1.*

The failing bit cell was scanned with the AFP. Figure 10 is the topographical image of the failing bit cell and Figure 11 is the corresponding current contrast image produced by the AFP. The current contrast image would indicate if any of the underlying Metal 1/contact/active interfaces were resistive. Since all Metal 1 lines are visible, a resistive interface was eliminated as a possible cause for the failure. Probing of the Metal 1 nodes was then performed to determine if there were any metal shorts between metal lines at the bottom of the Metal 1. Probing between the nodes of bit cell did not reveal any leakage and reconfirmed the lack of a resistive interface by producing normal diode curves through the connection of the Metal 1/contact interface to the underlying source/drain of the transistors.

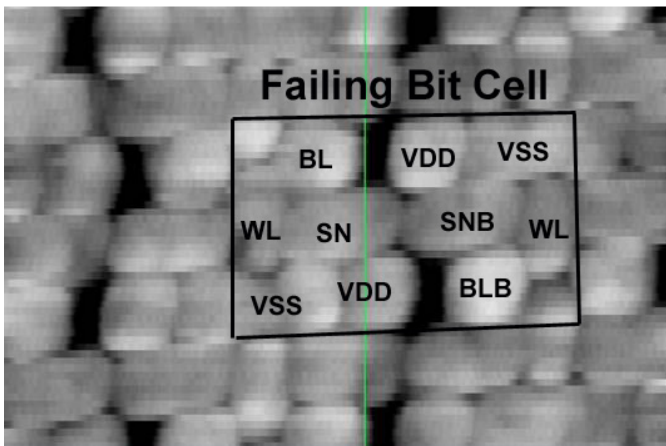

Figure 10: *Topographical AFP image of Metal 1. AFP probing of the adjacent Metal 1 lines within the failing bit cell did not indicate a short at the bottom of the metallization.*

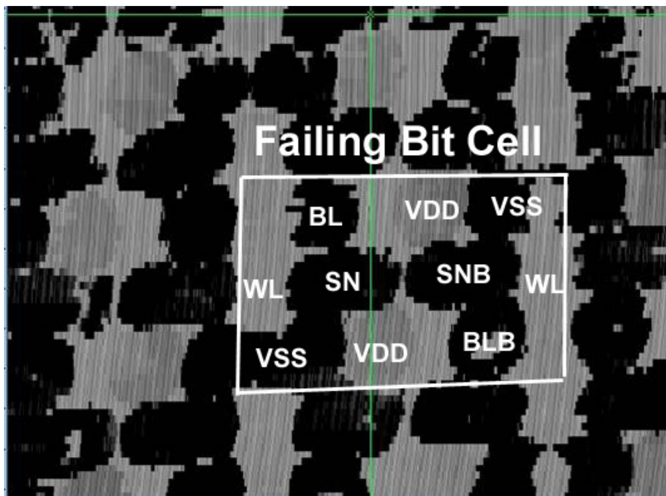

Figure 11: *Current Contrast AFP image of the Metal 1 layer. The results showed that the Metal 1 storage node(SN) lines do not have a resistive interface to the underlying contacts. The probing and current contrast imaging has eliminated a defect in the Metal 1 layer as the possible cause the bit cell failure.*

Based on this data, it was determined that there was no defect in the Metal 1 layer causing the single bit failure. The Metal 1 was then removed by mechanical polishing. The transistors of the failing bit cell were probed with the AFP [3]. The AFP results showed that the BLB p-channel transistor was faulty (Figures 12 and 13). Current conduction was minimal at low Vds levels. A TEM cross section analysis was performed on the faulty p-channel transistor, but no physical defect was found. However, the AFP analysis was successful in identifying the faulty p-channel transistor as the cause of the bit cell failure and was able to analyze the entire bit cell from the Metal 1 layer down to the transistor level.

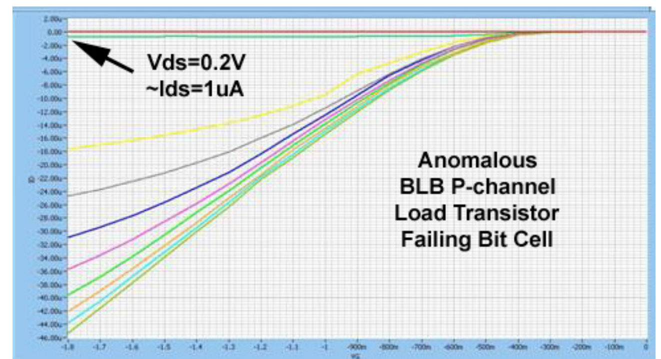

Figure 12: *Traditional AFP probing on the contacts found a p-channel load transistor in the failing bit had low conductivity at low Vds. Ids measured 1uA at Vds=0.2V.*

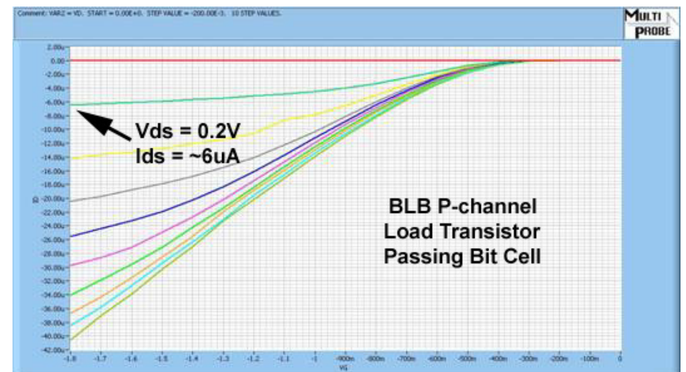

Figure 13: *Probing with the AFP on the contacts of a passing bit cell found that Ids measured 6uA at Vds=0.2V for the p-channel load transistors.*

Case Study II: SOI CMOS Current Contrast Imaging

Current contrast imaging of bulk semiconductor devices on the AFP is performed by scanning the exposed contacts of the transistors with the probe tips biased (and the well bias through the back of the die or using one the tips to bias the well at the well contact) and measuring the conduction through the tips as they make contact to the various features of the device [4], [5]. When the tips are touching oxide or one of the contacts connected to the gate of a transistor, a minimal amount of current is conducted through the tips. When the tips touch a contact connected to a source or drain of a transistor, significantly more current conducts due to the forward biasing of the source/drain to well diode. This information is then used to construct an image of the area scanned to allow the user to quickly evaluate if a transistor gate is leaky, or see a missing source/drain contact thatís not conducting (Figure 14).

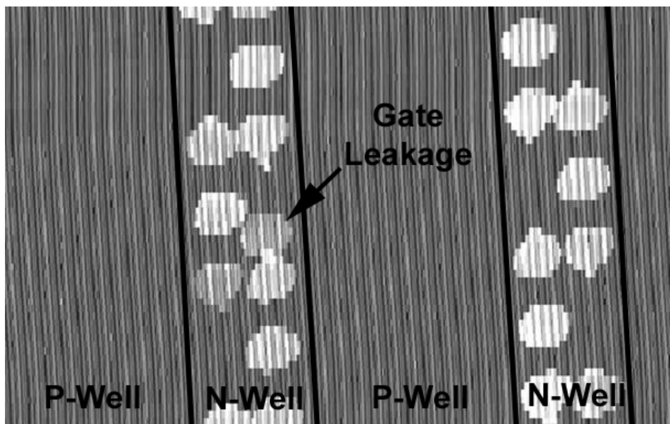

Figure 14: *AFP current contrast imaging of a bulk semiconductor device. In this image, the n-well has been biased to ground with one of the probe tips while another probe tip is biased with a positive voltage and scanned over the failing bit. The biasing causes current conduction through the source/drains of the p-channel transistors to the well. A gate contact is also visible due to a damaged gate oxide that allows for current conduction to the well.*

Another method to perform current contrast imaging is to use the optical microscope on the AFP to illuminate the area of interest with light while scanning the area with the probes biased to ground. The light causes the generation of photo-electrons in the silicon causing the active to be biased. This allows the tips to scan the area and measure the amount of conduction through the contacts without the need of manually biasing the wells (Figure 15).

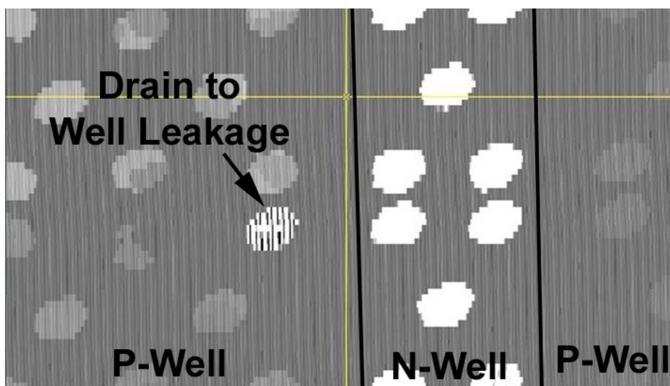

Figure 15: *AFP current contrast imaging of a bulk semiconductor device using the light on the microscope at high magnification to bias both the n and p doped silicon. The probe tips are biased to ground as they scan over the area of interest resulting in the conduction of current.*

This same technique can be used to perform current contrast imaging on SOI CMOS transistors. Although, technically there are no wells in SOI transistor technology, there is a small substrate region in the source/drain areas and under the gates. When exposed to the highest intensity of the microscope light at the highest magnification, this substrate region generates enough photo electrons to bias the source/drain junctions and allow enough conduction through the AFP probed tips to produce an image.

Figure 16 shows a current contrast AFP image of a 90nm SOI CMOS SRAM array containing a failing bit cell using the previously described method. In the image, a contact to one of the transistor gates is visible. This indicates that the contact is conducting current through the gate due to possible gate oxide damaged. AFP probing confirmed the gate oxide leakage, but TEM cross section analysis through the failing transistor did not find a defect (Figure 17). The information obtained by AFP analysis was sufficient to allow changes to be made to the gate oxide process in the wafer manufacturing facility thereby correcting the single bit failures.

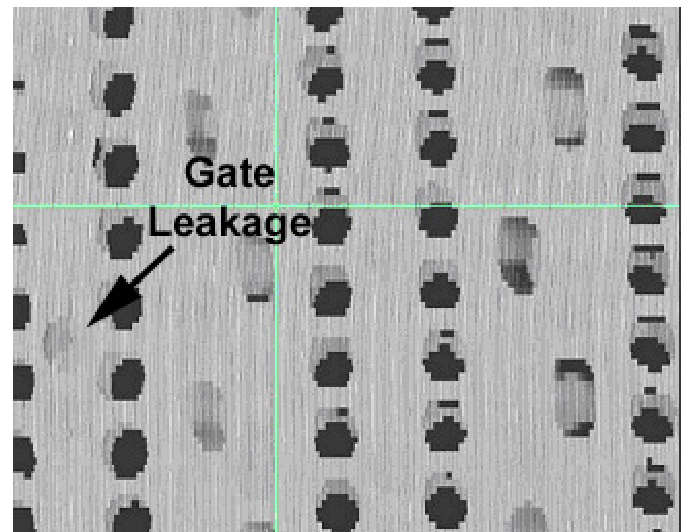

Figure 16: *AFP current contrast imaging of a SOI SRAM array using the light on the microscope at high magnification to bias both the n and p substrate under the gates. For this device, a gate contact is visible indicating leakage through the gate.*

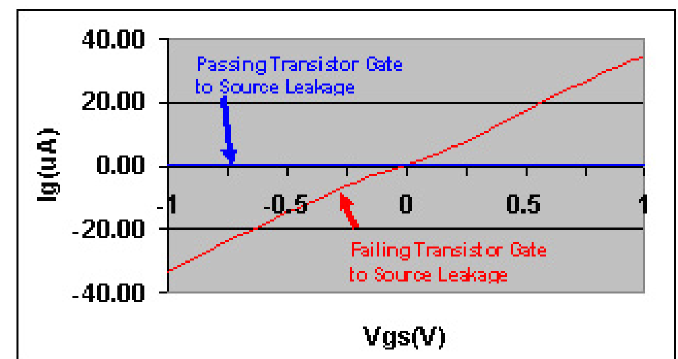

Figure 17: *AFP probe results for the gate contact shown in Figure 16 shows gate leakage to the source of the transistor.*

Case Study III: Light Emission and AFP Analysis

AFP analysis in conjunction with light emission analysis can significantly reduce the cycle time in analyzing failing semiconductor devices. Figure 18 shows a semiconductor device that failed due to high standby current. A light emission spot can be seen in one of the circuits. The circuit location generating the emission was identified. Tradition micro-probing was not possible at this location so the sample was removed from the package and deprocessed to the top of the contact layer. AFP current contrast imaging indicated a problem with the source and drain of one of the transistors (Figure 19). Probing and electrical analysis of the transistor found that the source was leaking to the well (Figure 20). SEM inspection of the transistor showed no defect even at the substrate level (Figure 21). Planar TEM analysis was performed and a dislocation was found in the substrate (Figure 22).

This case study demonstrates the power of AFP analysis in conjunction with light emission tools. Past analysis of light emission sights usually required several days of traditional micro-probing (FIB probe pads and micro-probe needles) if the probing was at all possible. AFP results were obtained in a single afternoon.

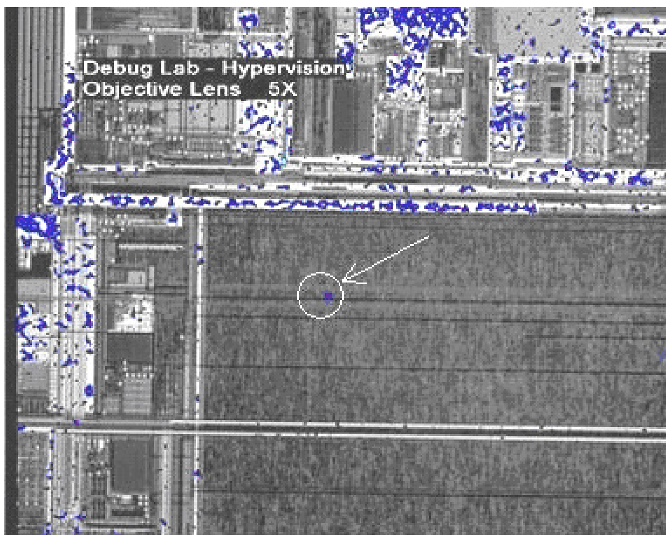

Figure 18: Light emission analysis identified an emission spot in the logic of a device that failed standby IDD. Light emission results provide by the Freescale Tempe Product Analysis Lab.

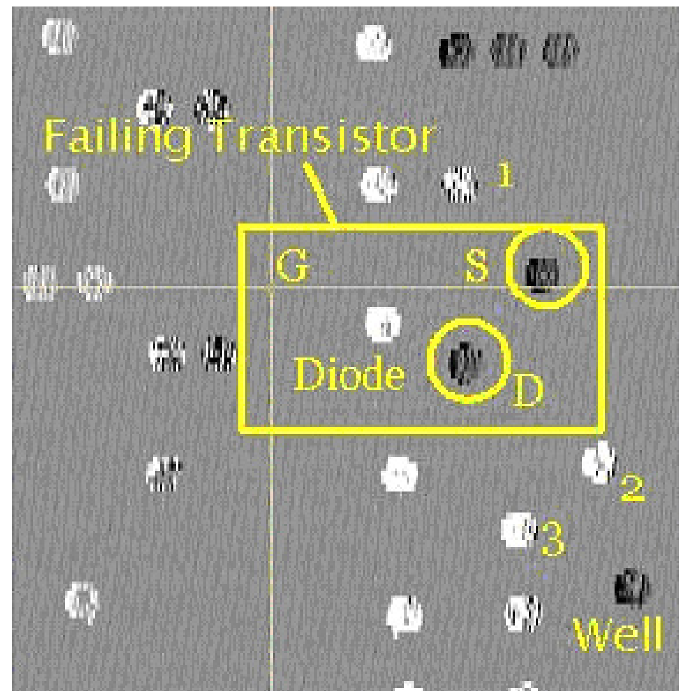

Figure 19: Current contrast AFP image of the transistor shows that the source/drain contacts for the suspect transistor had a different contrast than the surrounding source/drain contacts indicating that they were leaking to the p-well.

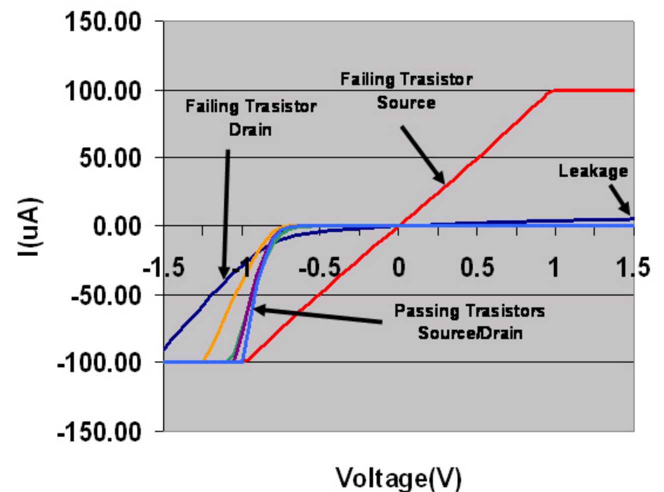

Figure 20: Two probe AFP measurements of the suspect transistor showed that the source and drain were leaking to the p-well.

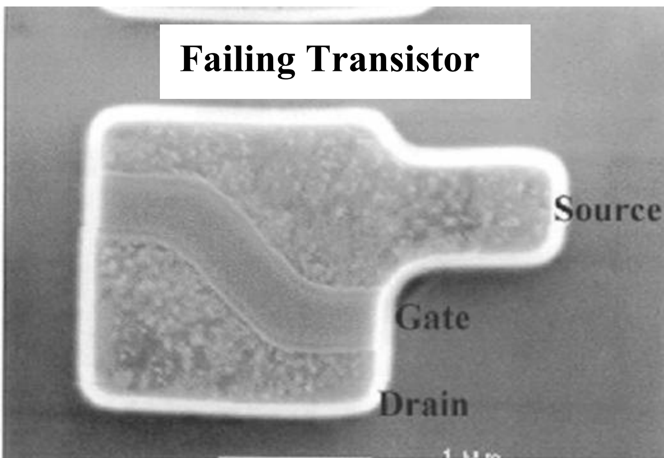

Figure 21: *The sample was deprocessed down to substrate and inspected with the SEM. No contact spike or silicide problem was found.*

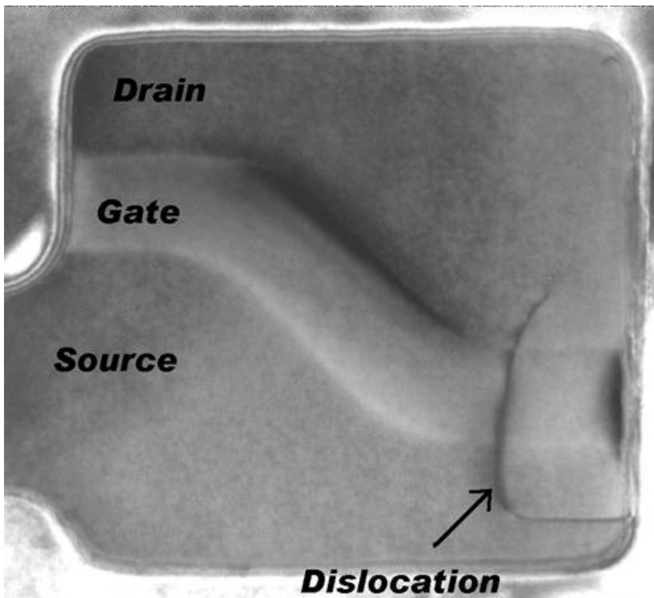

Figure 22: *Planar TEM image of the failing transistor shows a dislocation in the substrate that starts at the trench on the Source side and extends across the Gate to the Drain. This was the source of the light emission and the standby IDD failure. The combination of light emission, AFP, and TEM analysis resulted in the determination of the failure mechanism in a relatively short amount of time.*

Case Study IV: AFP Measurements on Copper Metallization

In this case study, the AFP was used to probe copper metallization lines of a 90nm CMOS DRAM device. The device had a double column failure. The column lines run adjacent to each other at the Metal 1 layer. It was thought that there was a short between the metal lines of the two columns. However, deprocessing and inspection at the wafer manufacturing facility did not find a metal short so a sample was submitted for AFP analysis to determine if the columns were shorted.

Figure 23 is the schematic for the DRAM columns. It was determined that AFP measurements could be made on the copper Via 1 plugs connected to the metal lines for the failing columns 51 and 52. The sample was deprocessed to the top of Via 1, but the sample was slightly over polished to the point where the remaining oxide above the Metal 1 lines was too thin to support the vias. The FIB was used to clear an area of the remaining oxide and expose the Metal 1 copper lines of the failing columns (Figure 25). The AFP was used to probe the metal lines (Figure 26 and 27). AFP results verified that one of the bit lines for each column was shorted to one of the bit lines for the other column (Figure 26 and 27). Probing on the metal lines for the adjacent passing column 50 and failing column 51 showed no short. Physical analysis of the failing columns did not locate the cause of the short, but it was demonstrated that the AFP could probe copper metallization and obtain electrical analysis results. It should be noted that copper vias can be difficult to probe. The copper vias can be damaged with just the probe force of the AFP tips pressing into them making it difficult to establish electrical contact. The copper metal lines appear to hold up better to probing which makes probing the metal lines more attractive than probing the copper vias.

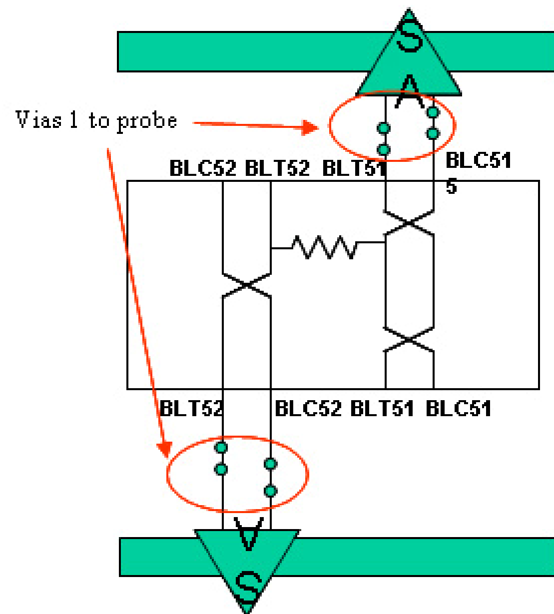

Figure 23: *Schematic of the DRAM columns showing the desired location to probe.*

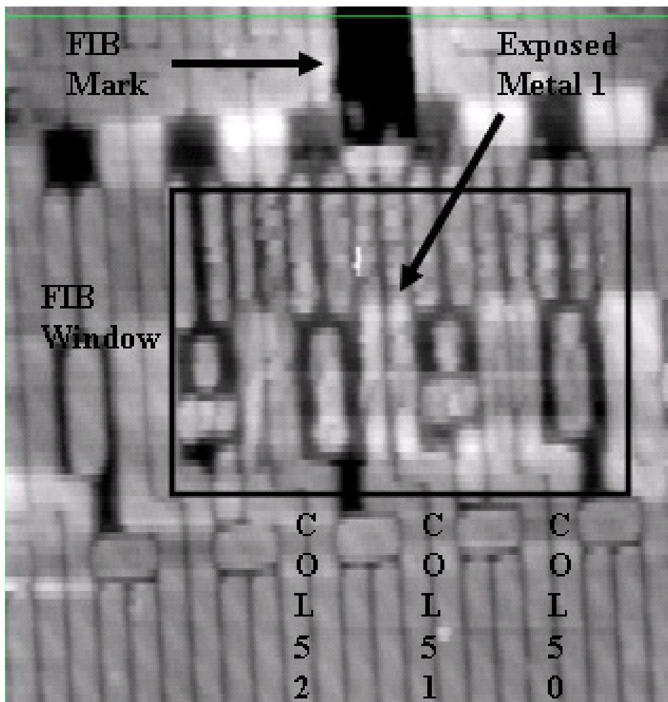

Figure 24: *AFP topographical image showing the failing columns 51 and 52 after the FIB was used to expose the Metal 1 lines.*

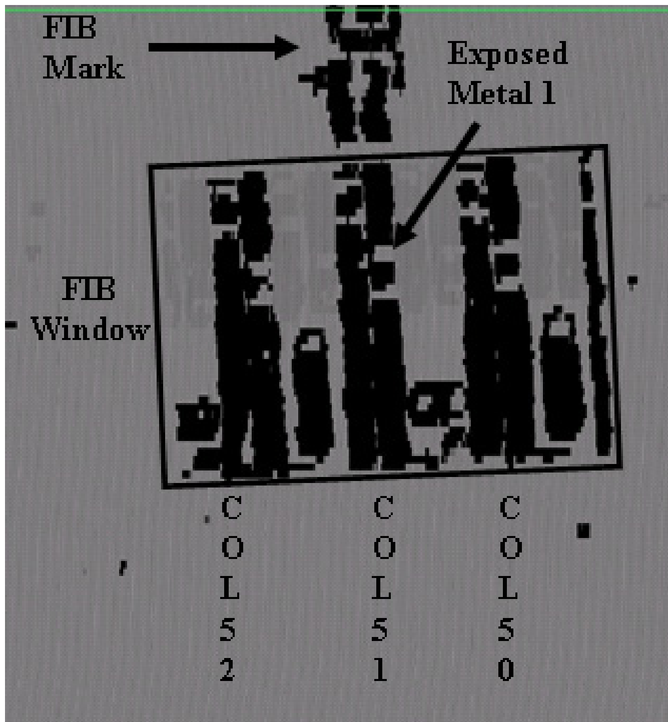

Figure 25: *AFP current contrast image showing the failing columns 51 and 52 Metal 1 lines are exposed and available for probing.*

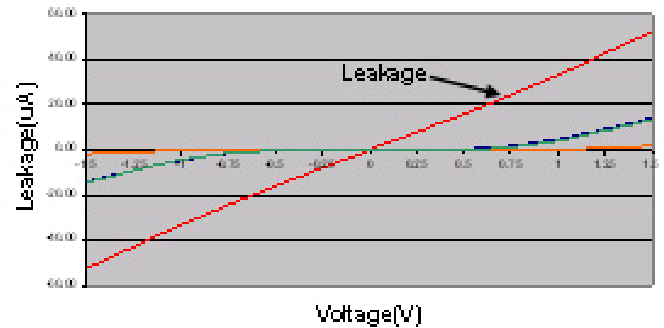

Figure 26: *AFP probe results shows leakage between Metal 1 lines of column 51 and 52.*

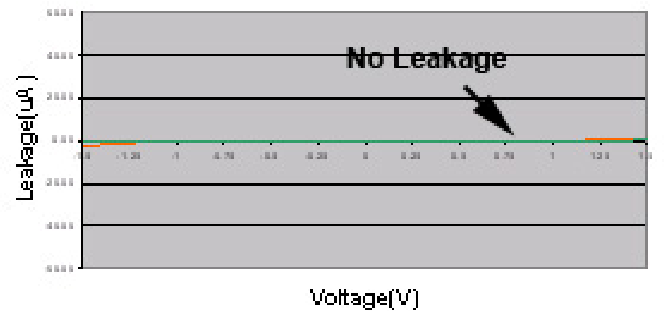

Figure 27: *AFP probe results showing no leakage between Metal 1 lines of column 50 and 51 compared to columns 52 and 52 in Figure 26.*

Case Study V: Surface Roughness Measurements

The AFP is a surface analysis tool that creates an image by measuring the displacement of the probe tip as it scans across the surface. The tool does have some capability to measure the roughness of a surface even though it wasnít designed specifically for that purpose. As the AFP scans over an area, it measures the deflection of the probe tip at numerous points along each scan line and the data is recorded. The tool is set to 100 data points per scan line and 100 scan lines per image. The tool takes the data for each scan point and constructs an image based on the measured deflection to the probe tip. Measurements can be made by making statistical calculations on the recorded data. The distribution is usually a normal distribution centered at zero after the data has been normalized (the zero point is relative during the scan). Measurements of the surface roughness can be estimated by looking at the full width at half maximum (FWHM) of the distribution.

In this case study, package lead-frames were submitted for surface roughness measurements. Lead-frames are the backbone of a packaged semiconductor device. The semiconductor device is glued on the flag of the lead-frame. Wire bonds are then attached from the bond pads on the semiconductor device to the lead fingers of the lead-frame. Finally, a mold compound material is pressed around the semiconductor device and the body of the lead-frame to form a packaged device. The lead-frame supports the structure of the package and electrically connects the semiconductor device to the outside world (print circuit board).

Lead-frames, which are made of copper, usually have a roughing agent sprayed on them to allow for the mold compound to adhere more strongly to the surface of the lead-frame. This roughing agent consists of an adhesive and particulates of a designated size. In this case, the size of the particulates was rated at ~2000 angstroms Package engineering requested that the size of the particulates be verified by measuring with the AFP. A lead-frame with no roughing agent was also provided for comparison.

Figures 28 and 29 show the lead-frames to be measured. The surface of lead-frame in Figure 29 appears bright due to the surface roughing agent that was sprayed on the surface. The flag of the lead frame was chosen as the location for measurement. The AFP tips were placed on the flag and a 15x15um box was scanned. The topographical AFP image of the surface roughness for each sample is shown in Figures 30 and 31, and the distribution for each scan is shown in Figures 32 and 33. The measurement of the surface roughness at the FWHM of the distribution for the sample with no roughing agent is +/-50nm. The measurement of the surface roughness for the sample with the 2000 angstrom roughing agent is +/-0.2um (or +/-2000 angstroms) which is a multiple of the expected size of the particulates in the roughing agent. This indicates that the particles are not in a single layer on the lead-frame but are stacked at least two layers high.

It was found the quality of these types of measurements is improved by making the scan area as large as possible and reducing the scan rate. However, doing so greatly increases the time to make a measurement so a trade-off has to be made between accuracy and speed.

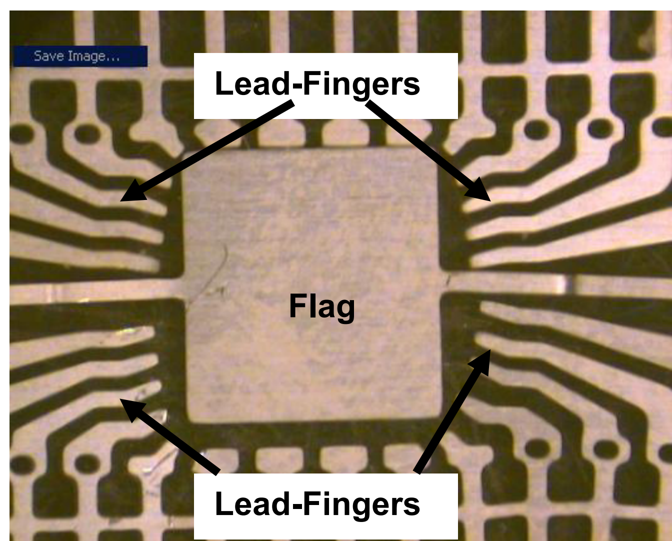

Figure 28: *Optical photo of a package lead-frame with no roughing agent sprayed onto the surface.*

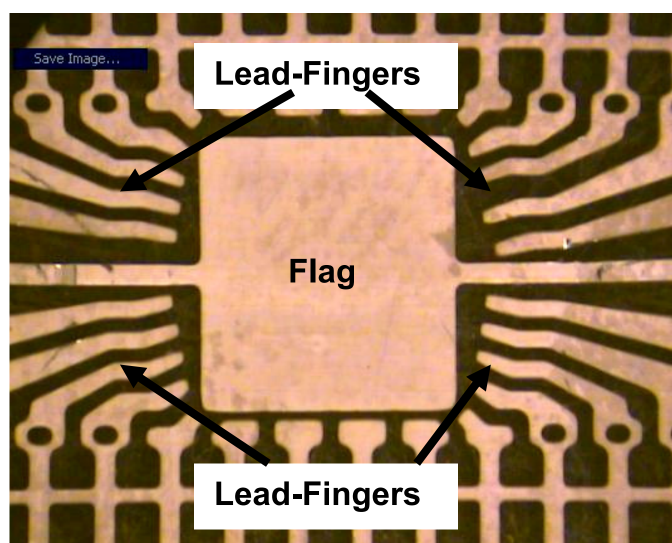

Figure 29: *Optical photo of a package lead-frame with ~2000A roughing agent sprayed onto the surface.*

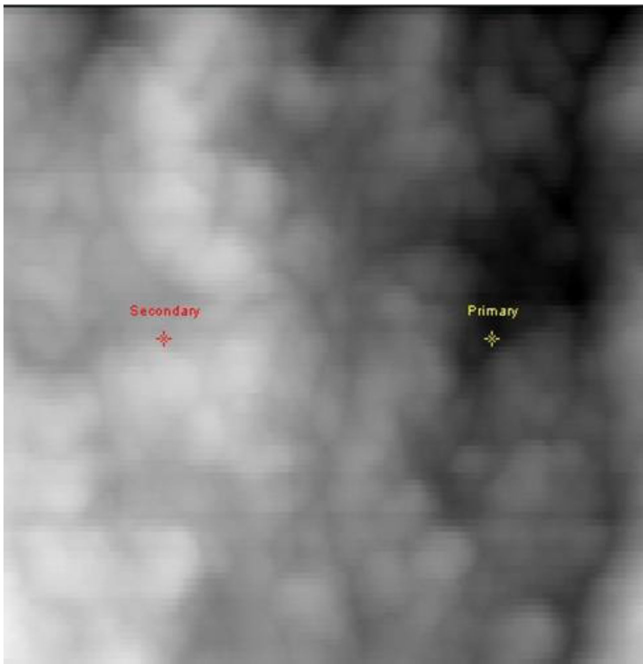

Figure 30: *Topographical AFP image of the lead-frame with no roughing agent.*

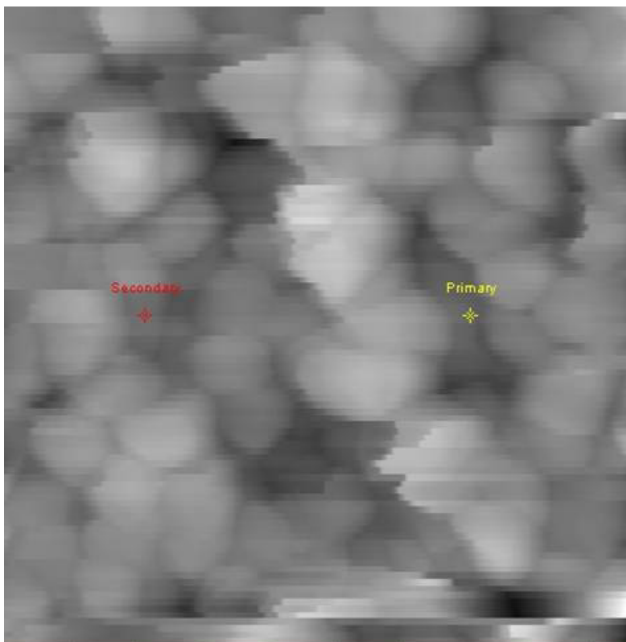

Figure 31: *Topographical AFP image of the lead-frame with 2000A roughing agent. The particulates can be clearly seen.*

Conclusion

In this paper, several case studies were provided to demonstrate the versatility of the AFP. The AFP was originally designed to probe and electrically characterize transistors at the contact layer. However, the needs and demands of the failure analysis environment have quickly

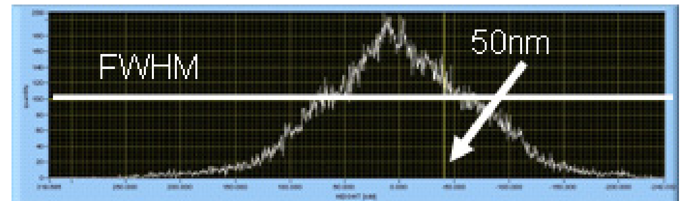

Figure 34: *The distribution of the AFP measurements at the FWHM point gives a measurement of +/-50nm for the lead-frame with no roughing agent.*

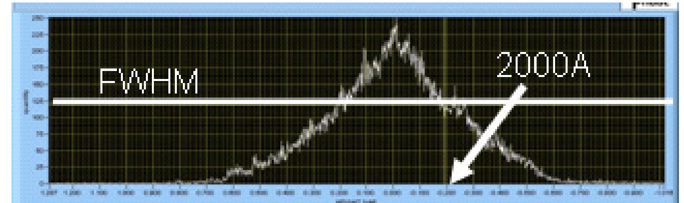

Figure 35: *The distribution of the AFP measurements at the FWHM point gives a measurement of +/-2000A for the lead-frame with the 2000A roughing agent.*

expanded its use. These expanded capabilities make the AFP more valuable for the failure analysis community.

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