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The Electrical Characterization and Physical Failure Analysis For Transistor Gate Leakage

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Introduction

Continuing advancements in semiconductor technology have meant device scaling to nanometer feature sizes and steadily increasing transistor densities. Killer yield defects in these nanometer sized devices can be submicron in size and frequently invisible

The emergence of advanced failure analysis has enabled the detection of these invisible defects more recently [1-2].

In this article, the electrical and physical analysis of gate leakage in nanometer transistors using C-AFM (conducting atomic force microscopy), nano-probing, TEM (transmission electron microscopy), and chemical decoration on simulated overstressed devices is described.

A failure analysis case study involving a soft single bit failure is first detailed. A suspected transistor with gate to source/drain leakage was isolated first with C-AFM, a method widely used for failure analysis of advanced semiconductor products. Nano-probing was employed to measure the electrical behavior of this individual device for further analysis. The Id-Vg behavior of this suspect transistor differed significantly as compared to a reference, non-failing device.

Exchanging the nodes of the source and drain while sweeping the voltage, the Id-Vg behavior of the suspect device was found to be similar to the reference device. However, an anomalous source to drain gate leakage in the suspect device was measured from the current components of the Ioff I-V plot. The asymmetry noted in the I-V behavior of the suspect device indicated that gate leakage was only present on one node of the source/drain region.

To confirm the hypothesis of source to drain leakage, the nano-probing results were compared to the simulation data for a source to drain leakage on this device. When this comparison was made, the nano-probing results matched the simulated Id-Vg behavior for a S/D gate leakage.

Following this nano-probing analysis, TEM cross sectioning of this failing device was performed. A local gate oxide anomaly was observed. Based on this analysis, another approach to further highlight the leakage point was implemented. A voltage bias was applied to exaggerate the gate leakage site.

Following this deliberate voltage overstress, a solution of boiling 10%wt KOH was used to etch decorate the gate leakage site followed by SEM inspection.

Methods and Analysis

For C-AFM and nano-probing measurement, DI Dimension 3100 and Hitachi N-6000 were used respectively in this case study. Failure analysis was performed on the SRAM soft single bit failure followed by C-AFM analysis as shown as Figure 1(a) and 1(b).

C-AFM current mapping shown in Figure 1(a) disclosed an anomalous signal in the SRAM contacts. Comparing the layout of the SRAM cell in Figure 1(a) with the C-AFM I-V measurements shown in Figure 1(b), it was suspected that a leakage existed between contact 2 and contact 1. The S/D gate leakage was present in one node only, indicated by the T1 transistor shown in Figure 2.

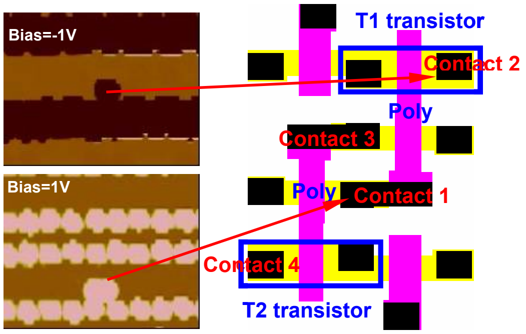


Fig. 1(a): The C-AFM current mapping and layout of SRAM cell. The abnormal contacts can be found from C-AFM current mapping.

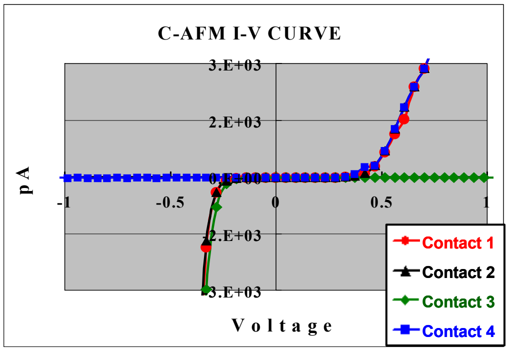


Fig. 1(b): The I-V curves measured by C-AFM. S/D gate leakage between Contact 1 and Contact 2 was suspected.

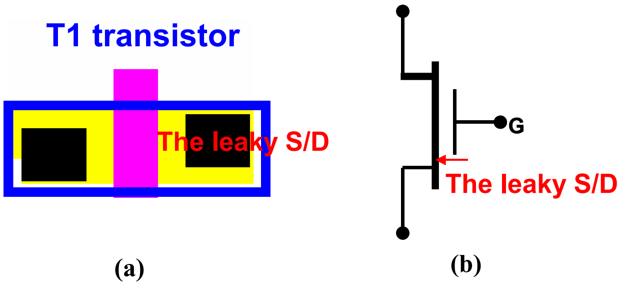
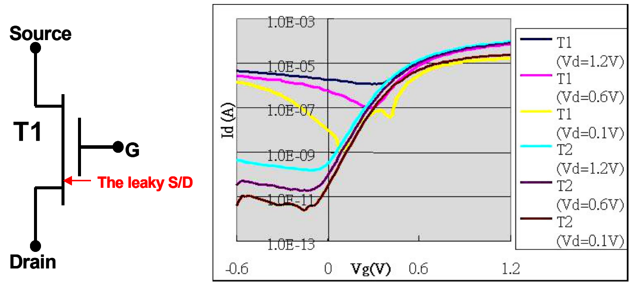


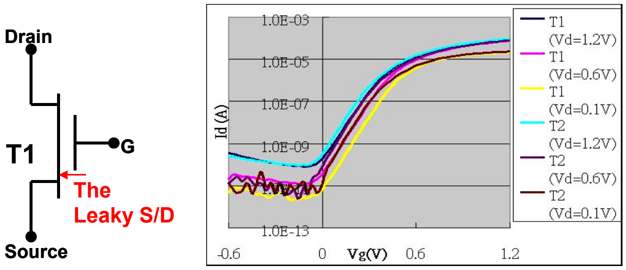
Figure 2: (a) The T1 transistor with one node S/D leakage was suspected from C-AFM data. The schematic is simplified as shown in (b).

For further analysis, nano-probing was used to measure the electrical behavior of the T1 transistor. When the leaky node was set as drain, the Id-Vg behavior of the T1 transistor was significantly different from that of the reference transistor T2 (Figure 3). Exchanging the nodes of source and drain, the Id-Vg behavior was similar between T1 and T2 transistors (Figure 4). Furthermore, S/D gate leakage in the T1 transistor was observed from the Ioff current components (Figure 5). The asymmetry I-V behavior meant that the S/D gate leak only happened on one node.



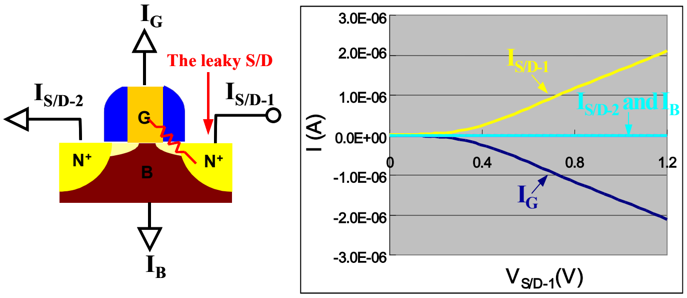
(a) **(b)**

Figure 3: (a) The Source, Drain (leaky side) and Gate of T1 transistor were illustrated for the nano-probing measurement. (b) The Id-Vg curves of abnormal transistor T1 and reference transistor T2 are shown.



(a) **(b)**

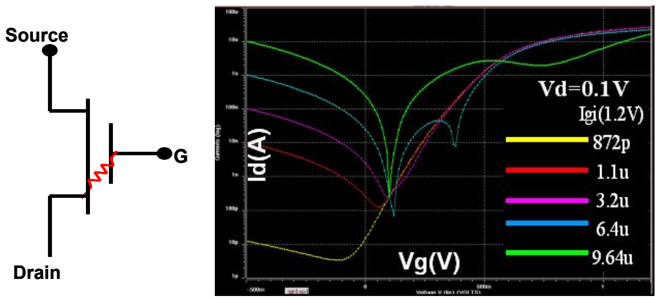
Figure 4: (a) Exchanging the S/D nodes, the Source (leaky side), Drain and Gate of T1 transistor are illustrated for the nano-probing measurement. (b) The Id-Vg curves of abnormal transistor T1 and reference transistor T2 are similar.



(a) **(b)**

Figure 5: (a) the current components I_G, $I_{S/D-1}$, $I_{S/D-2}$ and I_B of T1 transistor are illustrated for the nano-probing measurement. (b) The Ioff current components of T1 transistor show S/D gate leakage.

To further confirm the nano-probing result and verify the hypothesis of gate oxide leakage, a simulation of a S/D gate leakage was performed. The Id-Vg simulation behavior closely matched the nano-probing result shown in Figure 6.



(a) **(b)**

Figure 6: (a) the schematic of the simulation condition. (b) The simulation result shows the Id-Vg behavior nearly matching the nano-probing data.

A local gate oxide anomaly (thinning) observed from the cross sectional TEM images was believed responsible for the S/D gate leakage in transistor T1 (shown in Figure 7). Since the gate leakage site was small, a further approach to exaggerate the gate leakage site was pursued. A voltage bias over-stress was applied between the leaky gate and S/D node. Next, the voltage over-stressed sample was polished to polysilicide. Following this step, the sample was etched decorated in boiling 10%wt KOH solution and then SEM inspected.

A voltage over-stressed site was clearly visible at the poly edge (Figure 8). An anomaly in the gate oxide was highlighted which confirmed the suspected gate leakage in only one node of the S/D of the T1 transistor.

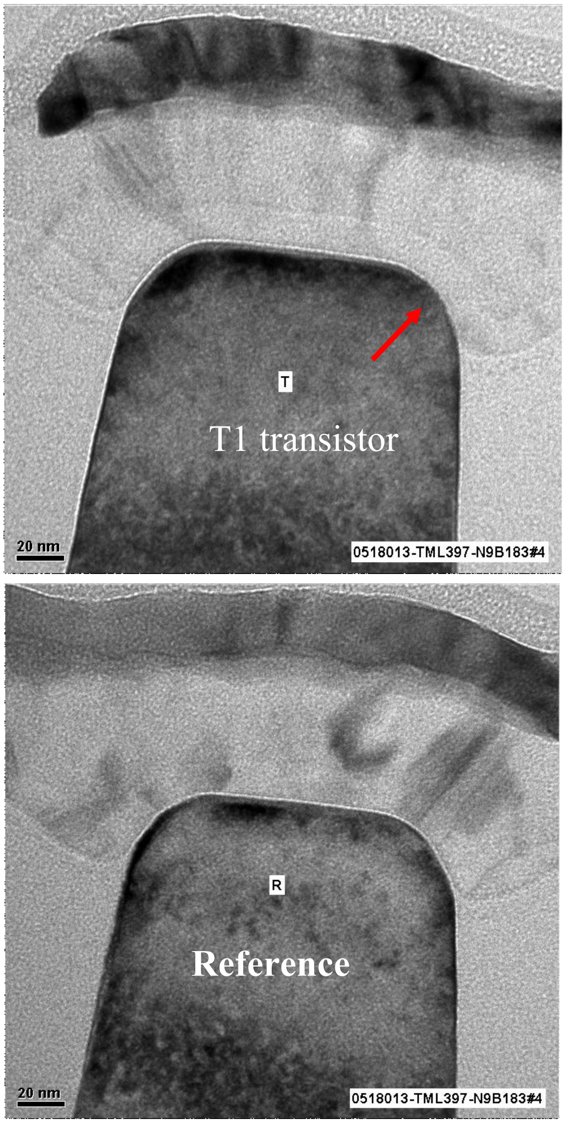


Figure 7: Tiny gate oxide anomaly (indicated by the arrow) was identified in the TEM image of the gate leakage-site of transistor T1.

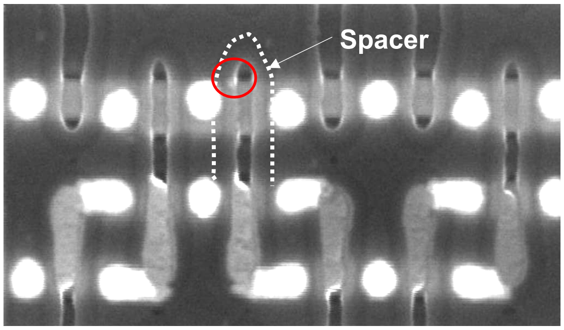


Figure 8: The overstressed site was highlighted following etching in boiling 10%wt KOH solution.

Conclusions and Acknowledgments

As device features scale down to nanometer range, non-visible defects such as gate leakage defects will become more frequently a source of failure. C-AFM and nano-probing will be key tools for the fault isolation and electrical measurements in these types of transistor failures

Different transistor leakage behaviors can be identified with nano-probing measurements and then compared with simulation data for increased confidence in the failure analysis result. Furthermore, nano-probing can be used to apply voltage stress on a transistor or a leakage path to worsen the weak point and then observe the leakage site easier.

References

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[2]. C. C. Wu, Jon C. Lee, J. H. Chuang, and T. T. Li " Single Device Characterization by Nano-probing to Identify Failure Root Cause", *Proceeding of the 31st International Symposium for Testing and Failure Analysis 2005.*

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