

## Atomic Force Probe Kelvin Measurements of Large MOSFET Devices at Contact Level for Accurate Device Threshold Characteristics

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### Introduction

As transistor geometries shrink into the nanoscale, the importance of nanoprobng is increasing. Most root cause failure analysis has relied upon the ability to use microscopy techniques to image defects in semiconductor structures. However, recent reports have indicated that standard SEM microscopy techniques, which have been the mainstay of FA labs, may become incapable of locating most defects at the 45nm node.<sup>1</sup> If the prediction is accurate, SEM microscopy may join a very long list of tools that have been relegated to tasks leading to, but not ultimately providing root cause. If it vacates the starring role it has held for 20 or 30 years, it will leave a far greater hole than any tool since the optical microscope!

However, there should be some comfort to the FA community in understanding the nature of defect signature detection. For instance, in each of the tools that analysts have come to depend upon, the method of detection, such as thermal IR microscopy, the signature (in these case photons is conveniently detected via some external means. We use those tools because they are fast and convenient, not because there are no alternative means of detecting defects. As the defect signatures become fainter and smaller, there is always one way that will never lose its effectiveness in detecting defects. Of course, this is referring to the electrical characteristic signature of the device itself. No matter what type of defect, it is the transistor device itself and its electrical signature which provides the best means of detecting a defect. By definition, there is always an electrical signature from the device itself. The objective for the analyst and the tool that is employed becomes characterizing the defective device with sufficient sensitivity and accuracy.

As has been covered in other papers, the methods for narrowing down the area of interest to acceptable size via fault localization are done with software, SEM or FIB passive voltage contrast (PVC), Optical Beam techniques, and more recently with current mapping.<sup>2,3,4,5,6</sup>

For most nanoprobng jobs, the robustness of circuit design insures that the defect signature is easy to detect. There would be no circuit failure unless the underlying device was almost not working. Therefore, the task becomes simplified to location of gross threshold mismatch, always on or always off

devices, or  $I_{d,sat}$  variations of 30% or more. These characteristics are relatively easy to find.

Unknown factors affecting these measurements such as probe tip contact resistance are either methodically removed<sup>5</sup>, or good and bad devices are compared to each other to compensate for measurement error. But low hanging root cause fruit is not always what we are looking for.

Nanoprobng at the contact level of MOSFET devices for accurate determination of true device characteristics (i.e.  $V_{t,sat}$ ,  $V_{t,lin}$ ,  $I_{off}$ ,  $I_{on}$ ,  $I_{d,sat}$ , etc.) is a growing concern in such peripheral logic circuits as SRAM and DRAM sense amps, PLL (phase locked loop ) circuits, and analog current mirror circuits. Each of these devices shares two similarities:

1. Circuit design is not as robust so that it is often necessary to either measure mV level threshold voltage characteristics or current drive measurements with 2- 3% precision.
2. These relatively large devices involve gate widths frequently exceeding 2 or  $3\mu m$  and gate lengths under 60nm and shrinking.

For nanoprobng of internal structures such as SRAM inverter transistors or internal DRAM transistors, the drive currents are much lower and failures tend to be more dramatic (easy to measure). As a result, small variations in contact resistance have little effect. Furthermore, the device is probed in a fashion similar to the way it is used in the circuit with one probe for each contact of the device.

In comparison, for large gate width devices such as those described above, a  $3\mu m$  gate width device will often involve 10 or more source as well as drain contacts.

To reconstruct discrete device threshold characteristics at tungsten contact level with AFP, specific care in making these measurements is essential. Kelvin probing (using two AFP probes for sense and two probes for force) as well as the proper placement of the AFP probes themselves is an absolute requirement for insuring precise measurements<sup>9,10</sup>

Although many claims have been made regarding tools providing the lowest contact resistance<sup>7,8</sup>, measurements of large gate width devices pose special challenges.

Kelvin nanoprobng with the atomic force prober combines low probe contact resistances in the low tens of ohms with the

ability to measure large devices ( $W > 3\mu\text{m}$ ) involving mV level threshold voltages and high drive currents with better than 2 to 3 % precision

This measurement precision is dictated not only on device geometry, but also on the spreading resistance in the silicide wiring, itself.

For the case of a sense-amp deprocessed to contact level, we have measured larger than 20% differences in saturation current due to the spreading resistance in the silicide of the source, based entirely upon where the contact is made.

For non-force/sense measurement, it is preferable to use the middle contact and to set the probes directly across the gate from each other. With this arrangement, at least 20 - 30% of the gate width will be receiving the correct voltage if contact resistance is ignored. An alternative approach would be to contact one extreme end, resulting in a doubling of the current spreading effect. The worst method would be to contact opposite corners of a device so that the voltage drop in the silicide is maximized and none of the device is biased at  $V_{dd}$ .

For this paper, NFET and PFET test structures employing  $3\mu\text{m}$  gate widths were used to simulate a sense-amp device. We compared the results obtained using normal pad-level probing on a conventional probe station with results from an Atomic Force Probe (AFP) nanoprobe with and without Kelvin sensing. These measurements are also compared with the nominal or expected design rule values.

## Method and Analysis

To evaluate the effect of Kelvin measurements with a five probe AFP tool on a large gate width MOSFET device, a PFET and NFET test structure was selected with a gate length of  $0.06\mu\text{m}$  and a gate width of  $3\mu\text{m}$ . Figures 2 and 3 describe this test structure at pad level. Figure 4 details the test structure at contact level, where AFP measurements were obtained. There are 15 contacts each on the source and drain and 8 on the gate.

Figures 5 and 6 are the threshold voltage plots obtained at pad level for the PFET test structure and for the NFET structure, respectively.

In order to measure the ‘as processed’ silicide resistance, a four probe measurement was carried out on the source and drain contacts. The sense probes were adjacent to and inside of the force probes. The force probes were on contacts 2 and 14 and the sense on 3 and 13. This means that the measured resistance is only the silicide from 10 segments and excludes the contact resistance and vias. Figure 7 describes the force and sense AFP probe placement for this resistance measurement.

From Figure 1, the silicide resistance is measured as 25 ohms per segment and the end to end resistance would be about 375 ohms. To put this into perspective, the benefit of a 10 ohm contact resistance would be dwarfed by the effect of the

silicide spreading resistance in more than 90% of the transistor!

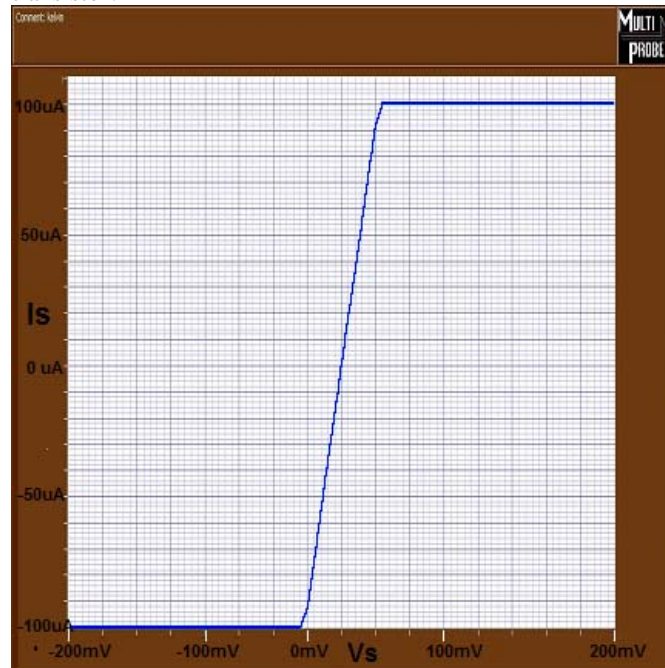


Figure 1: AFP 4 point measurements showing resistance of 10 segments of silicide on test structure.

The difference between conventional AFP probing and Kelvin probing is basically the silicide wiring distance that separates the tungsten contact vias for the device of interest. For an SRAM cell, the silicide wiring distance for gate/source/drain is less than  $2\text{nm}$ . In that instance, silicide sheet rho resistance effects are negligible. For large gate width devices as described in this paper where  $W > 3\mu\text{m}$ , Kelvin probing is required to null out the silicide sheet rho resistance effects.

For conventional pad probing, [Kelvin probe methodology] will only zero out the resistance in the copper metal to tungsten needle resistance and therefore is usually not employed because this resistance is thought to be very low. There should be very little resistance in the copper lines connection to the tungsten vias to silicide. The copper conductivity is in parallel with the silicide resistance and therefore, the measurements are taken as the ideal case. Nevertheless, the values deviate significantly from the nominal prediction especially as shown for PFETs in Table 1. This variation is believed to be process dependent, however.

In the case of Kelvin probing of devices, the most important node is that of the source, with the drain being less important. The importance attached to the source node comes from the gate voltage drop reduction that comes if the source is not at true ground potential but ‘floats’ up on the voltage drop across the probe contact resistance in series with the source silicide spreading resistance. The gate probe typically draws no current unless there is a problem, so that even large contact resistances have no impact.

The ideal case is to place two probes on each the source and drain and one probe on the gate. In this structure, no well contact is required since the device is Silicon-On-Insulator (SOI). Now the placement of the probes for measurement is equally important and unless care is taken, the benefit of the force/sense arrangement only extends to zeroing contact resistance and does nothing to combat the cumulative effect of the silicide. For instance, in the worst case, two adjacent contacts would be chosen as force sense. Because the sense probe serves the bias condition on the force probe, the voltage will be correct only at the position of the sense probe. Therefore, if the probes are adjacent, the portion of the S/D 'downstream' in the current path will suffer from the voltage drop in the silicide and the measured current will be lower resulting in lower  $V_{t_{sat}}$ .

If on the other hand, opposite corners of the device are chosen, the voltage drop across the entire length of the device will result in 90% of the device being exposed to a higher than correct voltage and measured  $I_{d_{sat}}$  higher and  $V_{th_{sat}}$  lower. If not carefully considered, the seemingly trivial placement of probes can result in large errors: If we assume case 2 of opposite corners and an  $I_d$  of 1mA, the voltage difference across this device would be about  $(0.001A)(375ohms) = 375mV!$

The best case is chosen with the possibly poor assumption that the silicide resistance is constant down the S/D. If this is the case, the best placement of probes is with the force probes directly across with the sense probes two thirds to three quarters of the way on the line of tungsten contacts. Since the resistance is assumed mirror symmetric around the force probe, the sense probe serves as the bias on *both* sides of the device and the error is reduced.

Nevertheless, great care must be taken in choosing not just the measurement method but also the location of the nanoprobe placement to minimize errors. When attempting to minimize errors on a structure such as this, it appears that far more important than the absolute contact resistance is the ability to place the force and sense probe on exactly the right location! This surprising result is clear when each of the three factors (silicide or implant resistance, probe placement, and  $I_{d_{sat}}$  levels) affecting the measurement is considered.

For the Kelvin-sense measurements on this structure, the force probes were on contact 8 and the sense probe on 3. This is shown in Figure 8.

Table 1 shows a comparison of the AFP/Kelvin probing and conventional metal pad probing. In 3 of 4 cases, the data from the AFP is closer to the expected value with the 4<sup>th</sup> data being almost identical. The relative merit in having values closer to expectation is not known and may be more coincidental than demonstrative. Nevertheless, the current values are within 2% of the pad values over the entire curve and as expected, were far superior to the non-Kelvin measurements.

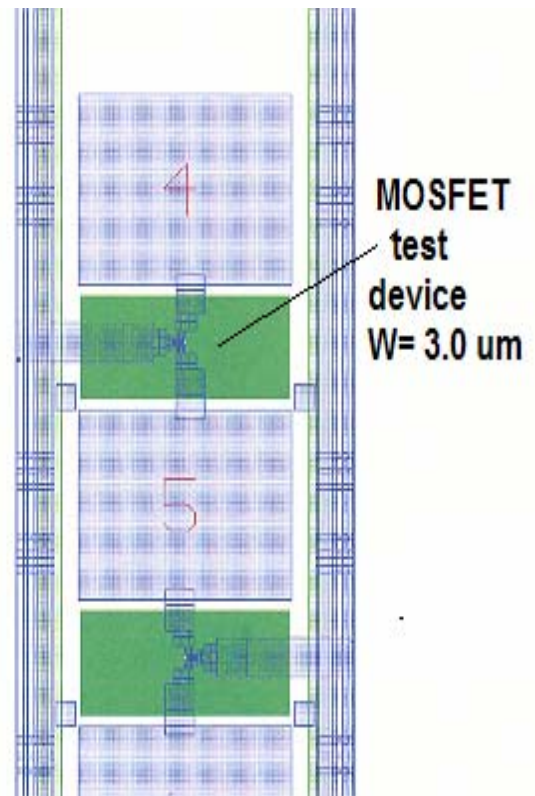


Figure 2: MOSFET test structure at pad level with gate width of 3µm and gate length of 0.06µm.

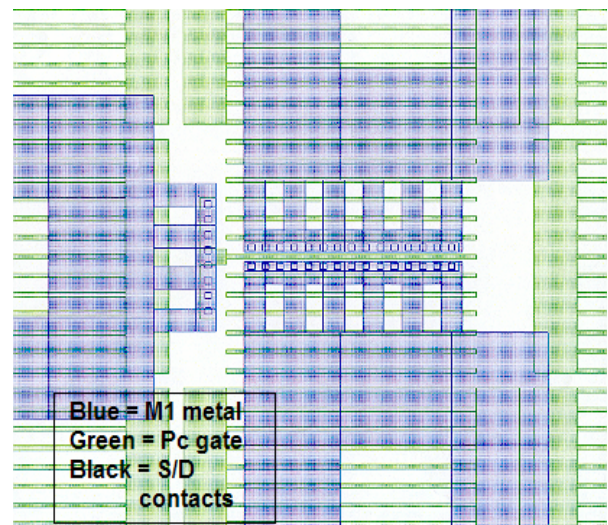


Figure 3: Detail of MOSFET test structure at pad level showing polysilicon gate, tungsten source drain contacts and M1 level wiring. PFET and NFET devices are identical in layout

Conventional probe pad electrical measurements were performed on this test structure and threshold measurements obtained for both devices.

Figures 5 and 6 show the threshold voltage measurements obtained by conventional probing at pad level for the PFET and NFET test devices.

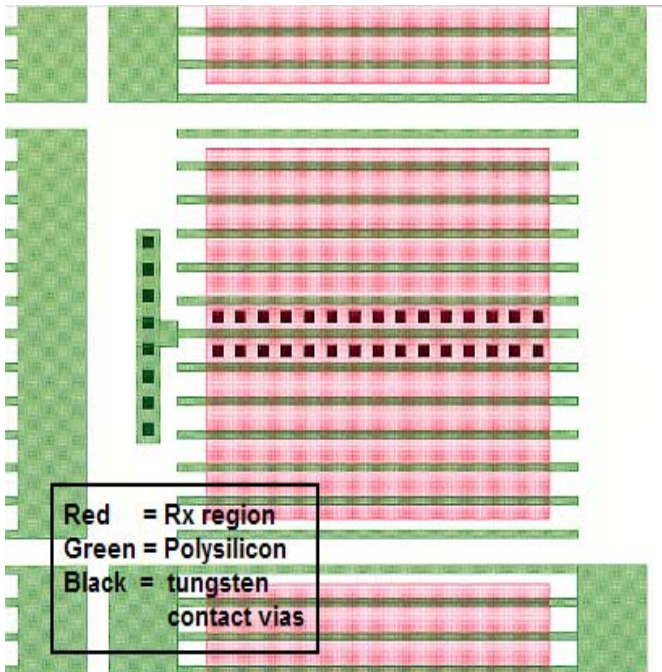


Figure 4: MOSFET device with gate width of 3µm and gate length of 0.06µm shown at contact level for AFP Kelvin measurements.

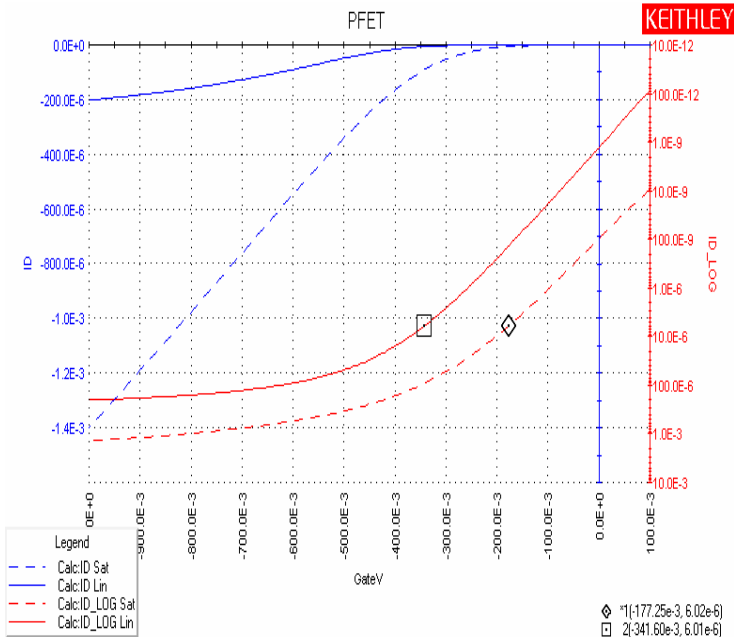


Figure 5: Threshold voltage measurement at probing pad level for PFET test structure device.

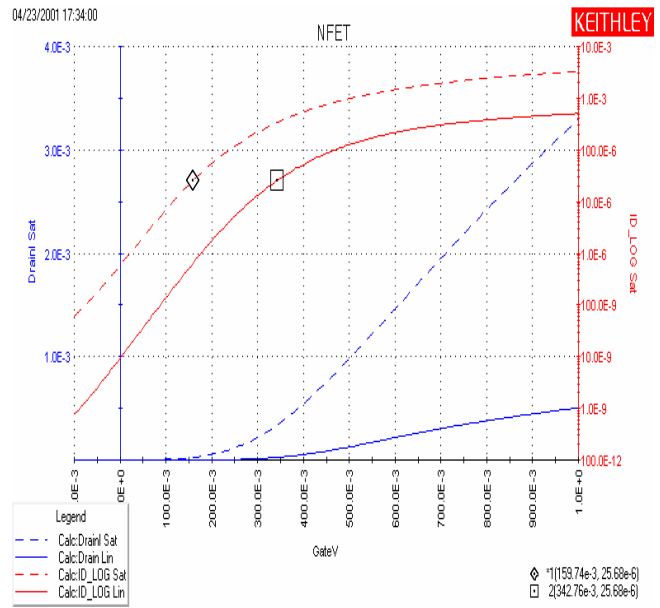


Figure 6: Threshold voltage measurement at probing pad level for NFET test structure device.

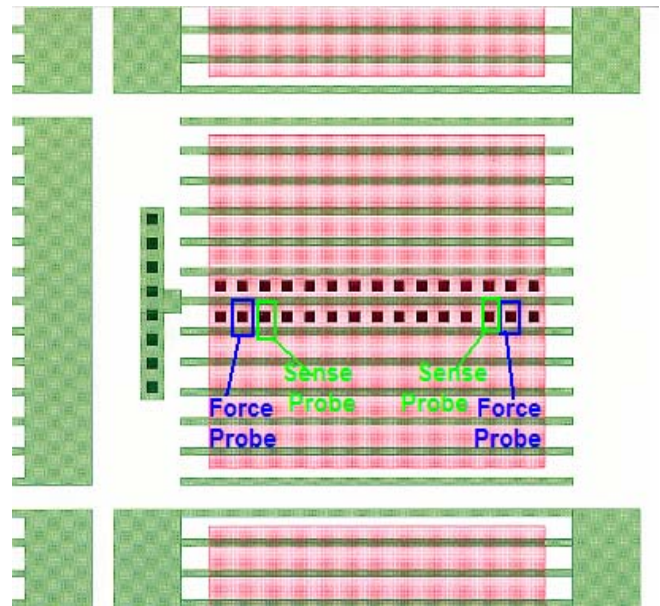


Figure 7: To measure “as processed” silicide resistance, location of four Atomic Force Probes are shown.

Silicide segments are between these probe nodes. Approximate AFP silicide resistance indicates a silicide sheet resistance of 25 ohms per square.

Using a novel method of placement of the atomic force probes, true Kelvin measurements were obtained. Figure 8 shows this placement of the two AFP force probes and the two AFP sense probes.

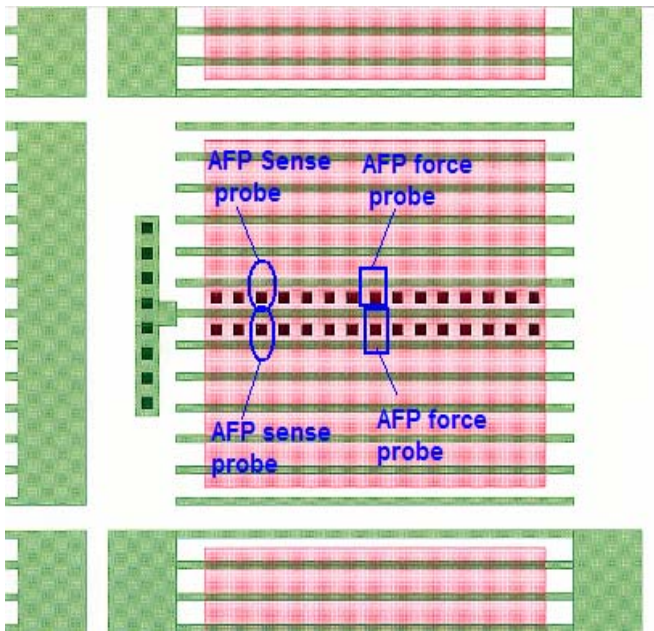


Figure 8: Kelvin measurements obtained by thoughtful placement of Atomic Force Probe tips, enabling symmetric biasing of the device. The silicide resistance voltage drop should be equivalent on both sides of the device.

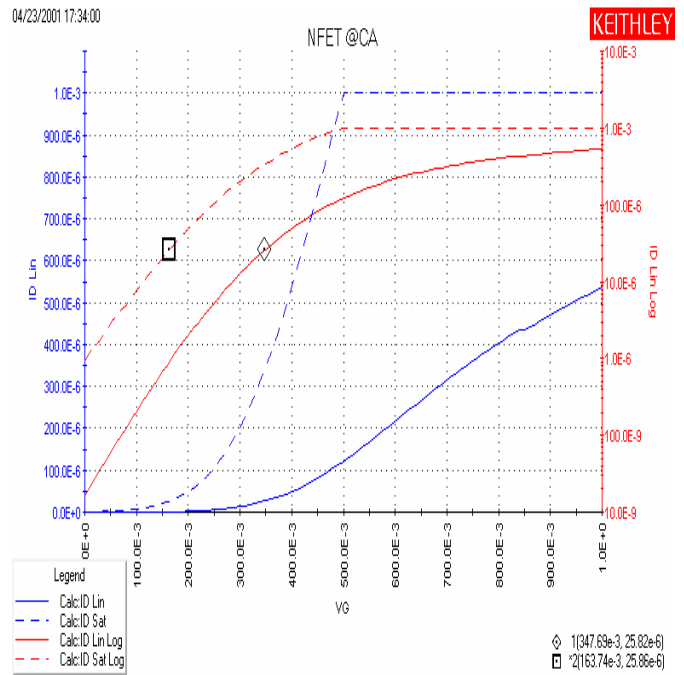


Figure 10: AFP Kelvin measurements of NFET test structure showing threshold voltage characteristics

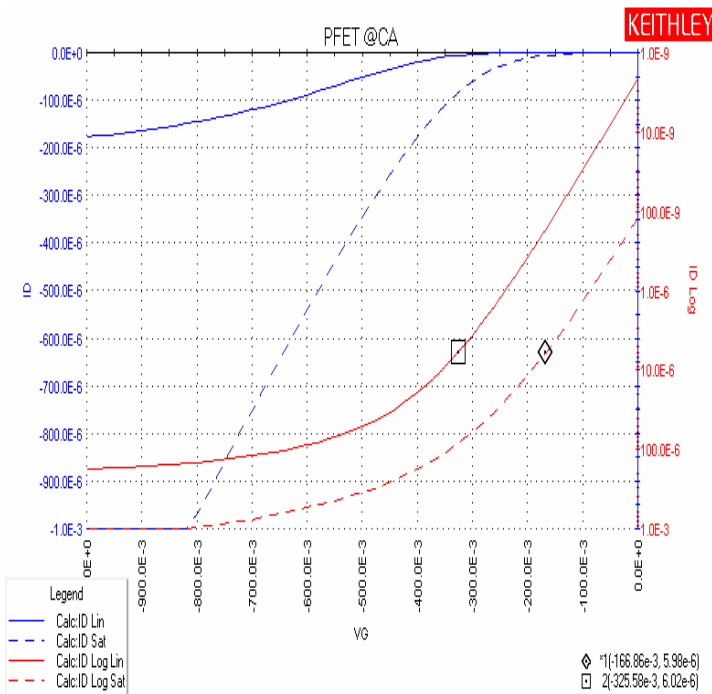


Figure 9: AFP Kelvin measurements of PFET test structure showing threshold voltage characteristics performed at contact level.

A comparison of the AFP Kelvin device measurements for  $V_{t,sat}$  and  $V_{t,lin}$  with the corresponding pad level measurements are detailed in Table 1, including the expected technology characteristics. The difference between expected PFET values and the measurements obtained by AFP Kelvin probed measurements and pad level measurements are due to process dependent variations.

	Nominal Device Characteristics $W = 3.0\mu m$ ; $L = 0.06\mu m$	AFP Kelvin Measurements at Ca contact level	Pad Probe Measurements
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NFET $V_{t,sat}$	160 mV	163.7 mV	159.7 mV
NFET $V_{t,lin}$	350 mV	347.7 mV	342.8 mV
PFET $V_{t,sat}$	130 mV	166.9 mV	177 mV
PFET $V_{t,lin}$	300 mV	325.6 mV	341 mV

Table 1: Detail of test site device measurements by Atomic Force Kelvin Probing and Pad Level probing measurements.

## Conclusions

Nanoprobing will continue to provide a method for determination of root cause even when all other microscopy techniques have ceased to be effective. Accuracy and sensitivity need to be improved through careful probing methodology; not simply to mitigate probe contact resistance but also to minimize errors due to voltage drops in the device.

The need to characterize large gate width MOSFET devices at contact level is an increasing concern for such peripheral logic circuits as SRAM sense amps, PLL circuits, and analog current mirror circuits where gate width features frequently exceed 3 $\mu$ m.

Experimental results comparing AFP Kelvin measurements at contact level on the same MOSFET test structure versus measurement obtained conventionally at pad level underscores the importance and value of AFP Kelvin measurements. The values obtained from the AFP were in most cases closer to the expected values for the devices than the conventional measurement. Confidence in the validity of the AFP four probe Kelvin measurements at contact level of these large MOSFET devices is a necessary requirement in order to reconstruct such device characteristics as  $V_{t,sat}$ ,  $V_{t,lin}$ ,  $I_{off}$ ,  $I_{on}$ , and  $I_{d,sat}$ .

For large devices such as those referenced in this paper, it is shown that probe location is at least as important as probe pressure. Therefore, it seems that for such devices, the most important requirement is resolution and accuracy over simple contact resistance.

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