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Combination of SCM/SSRM analysis and Nanoprobing technique for soft single bit failure analysis

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Abstract

Traditionally, many semiconductor companies have used SRAM memory to develop their process technologies. The job of the failure analyst is often to physically deprocess the sample and hope to find the defect with only the bit map location to guide them. The success rate has been better in the past when the size of these SRAM cell were bigger. With the technology shrinking every 2 years, the chance of finding physical defects has become less and less. Besides the shrinking SRAM cell geometries, the electrical failure signature for many of the failures is marginal (soft failure), presenting difficult challenges for failure analysis (FA). Physical analysis of these soft SRAM failures at the sub-100nm technologies is often non-visual without detailed isolation and electrical characterization. Therefore, additional techniques are needed to improve the successful FA on newer technologies. In this discussion, we will present the uses of both SCM/SSRM (scanning capacitance microscopy / scanning spreading resistance microscopy) analysis and nanoprobing technique for fail site isolation.

Introduction

In the past, ATE bit map data was usually sufficient for fail site isolation when dealing with DRAM or SRAM memory cell failures. These memory cell failures can be categorized as row, column, multiple bit, double bit or single bit signatures. The failure analyst can go to the failing bit(s) as long as the row and column mapping is correct. The traditional physical characterization method is to remove the layers of metal and dielectric from the failing location and inspect with Scanning Electron Microscope (SEM). This method is still sufficient for some hard failures caused by particles, missing contact or gross patterning defects. However, SEM inspection alone has had very low success rate to resolve soft failures.

A single bit failure is categorized as soft failure when it fails intermittently or only marginally. A good memory tester is capable to determine how a bit failure behaves. It can check the voltage and frequency range. It can find out whether it has write or read sensitivity. It can also verify if it has data retention or disturb issues. The more electrical data that can be collected, the better the hypothesis can help target a successful FA. However, an educated guess at the fail scenario followed by "blindly" looking around very seldom resolves these failures.

Based on SRAM cell layout, the most of essential component that would cause single bit soft failure is at contact level and below. A typical 6 transistors SRAM cell arrangement is with 2 loads, 2 driver and 2 pass gate transistors (see figure 1). When one of the transistors is not functioning, the electrical test will identify it as a single bit failure. A single bit failure can be classified as a hard or soft bit failure. A soft bit failure typically only fails at certain voltages or frequencies. The soft failure signatures are most common when the new technology process is still maturing and transistor performance is below design targets. A common soft failure can be attributed to imbalance or asymmetrical problem inside a single SRAM cell. The conventional techniques of SEM passive voltage contrast and top down SEM inspection are extremely limited to identify transistor related problems. When the top down SEM analysis fails to identify a fail mechanism, one has to try other techniques which target a portion of the failing cell such as TEM or backside silicon etching. These techniques are not always successful to identify the failure mechanism since the fail site has not been isolated to a particular node of the bit cell. This paper will demonstrate the successful use of SCM/SSRM and internal nanoprobing of soft bit failures which enabled the failure analyst to understand the electrical behavior of the transistors and pin-pointing the failing location prior to attempting physical failure analysis (PFA).

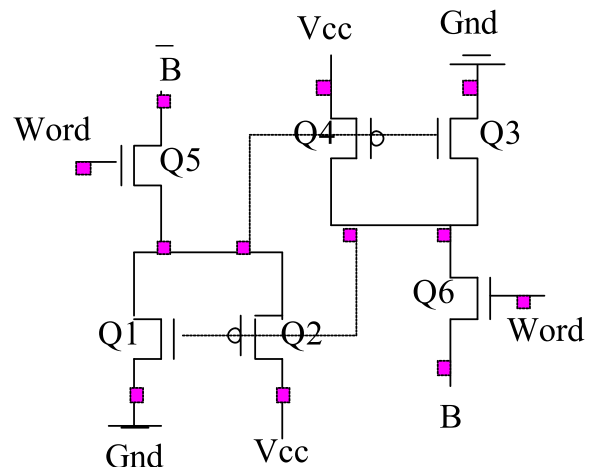

Figure 1 A typical layout of a SRAM cell with 6 transistors and 12 contacts.

SCM/SSRM Analysis

SCM and SSRM are traditionally used to characterize two-dimensional dopant profiles (for typical microelectronics applications, see Ref. [1]). We have found that SCM and SSRM [2] techniques can also be used as a single-probe "nano-prober" for isolating SRAM defects at the contact level. To do this we used etched W probes [3] in place of the metal-coated Si probes traditionally used in SCM. In this configuration, the contacts act as the extension of the conductive tip. Figure 2 shows an SCM image on a sample around a failing bit (we will call this a sample A). The cross sectional profile along the dashed line in Figure 2 shows that the dc/dv signals at the source and drain contacts of an NMOS in the fail-bit to be over twice dc/dv signals on the other NMOS in the other source and drain contacts (see Figure 3a). We also measured currents from the contacts to the substrate (by switching sensors) at fixed tip-sample bias using SSRM. The currents on the two source-drain contacts with dc/dv anomaly are the same. The magnitudes are about twice the average leakage current of the other reference source drain contacts when the tip voltage is 1V (see Figure 3b). Both the SCM and SSRM results lead us to conclude that the source and drain in this sample are shorted together. The normal SCM and SSRM signals measured on the gates indicate that neither source nor drain is leaking to the gate electrode.

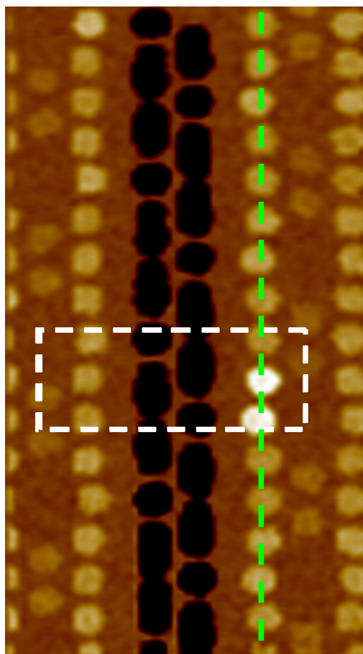

Figure 2. A top down view of SCM image which show abnormal brightness on two contacts on sample A.

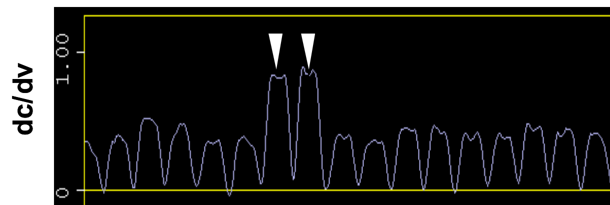

Figure 3.a SCM profile shows the dc/dv SCM signal is >2X on the two NSD contacts.

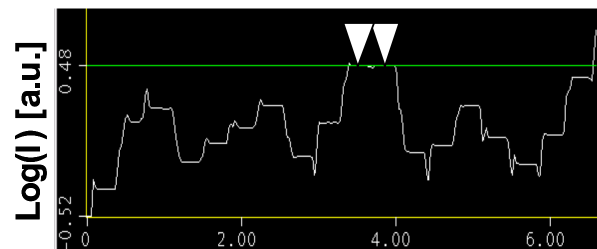

Figure 3.b SSRM profile shows the leakage through the two contacts is identical at reverse bias.

Nanoprobing technique

Since SCM/SSRM is non-destructive, an analyst can proceed with additional analysis. A SEM based probing system was used in this analysis [4] (see Fig. 4). We were able to navigate four probe tips and land them on a source, drain, gate, and well contacts. A family of I/V curves were collected on the good and failing transistors. After reviewing the IV curves and comparison with the reference good bit, we confirmed a 50 kOhm short between source and drain of the suspect transistor (see Figure 5). This result was consistent with SCM finding of source to drain short at the right side driver transistor. With the failing transistor isolated, additional physical analysis was targeted at this component to understand the root cause.

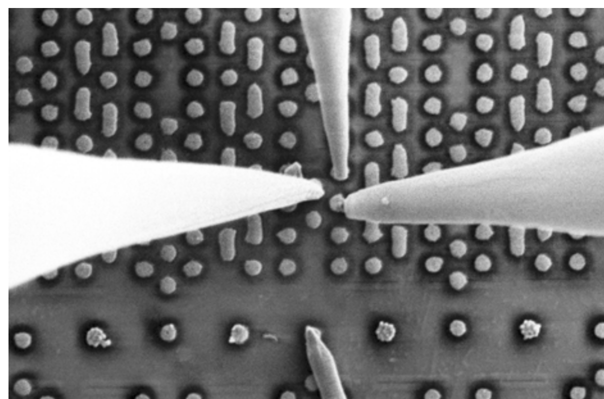

Figure 4. This figure shows four probe tips touch down on the source, drain, gate, and the well of a single transistor.

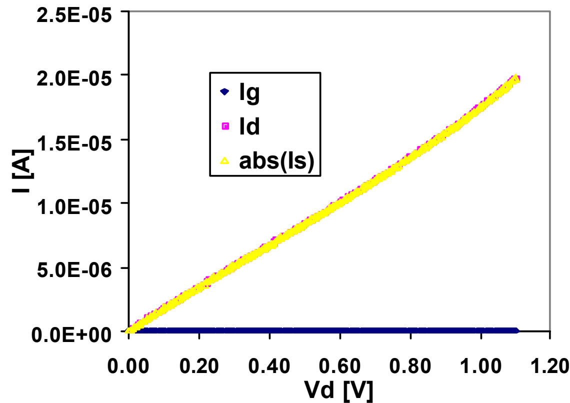

Figure 5. Nanoprobing of a single NCH transistor shows 50k ohm resistance between the source and drain contact.

Once SCM/SSRM and nanoprobing have isolated the failure to a particular transistor, the analysts can plan a deterministic physical analysis approach. In this particular case, a TEM cross section was performed at the failing transistor. The result showed that the source-drain leakage was due to a small silicon dislocation in the channel (see figure 6) [5]. This defect was previously non-visual by top down SEM and other FA methods since silicon stains are too aggressive for such small surface dislocations and small geometries.

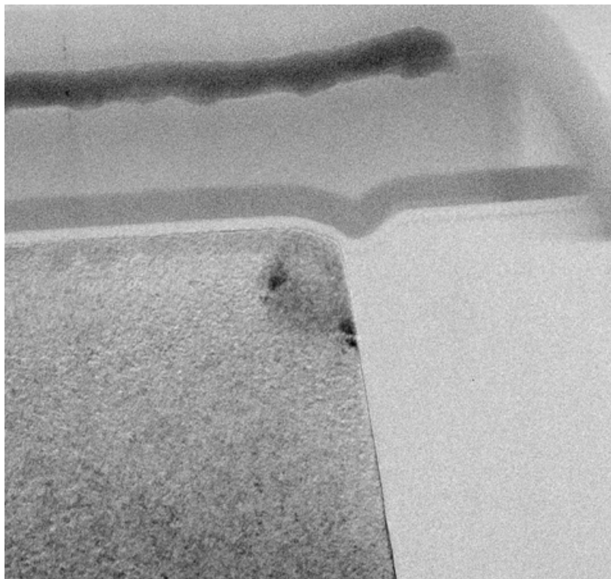

Figure 6. TEM cross section finds a dislocation at the edge of the transistor channel.

Additional Case Studies

The above sample A demonstrated the successful usage of both SCM/SSRM analysis and nanoprobing technique to identify the failure site which was previously non-visual by blind inspection. With additional samples and case studies, we recommend having both techniques available for fail site isolation since one of the techniques might not yield useful data, such as the case for the second case study (sample B).

Sample B

In the case of sample B, the problem was a Vmin sensitive single bit SRAM failure. Top down SEM analysis was not successful to identify the root cause. Unlike sample A, SCM analysis was also unable to identify any problems or isolate a bad transistor. Nanoprobing at contact level was required for successful fail site isolation. Based on the electrical data collected from nanoprobing, the left driver transistor was noted to exhibit with excessive resistance in one direction (asymmetrical Ion behavior). Once the failing transistor was identified, a TEM sample was prepared to understand the asymmetrical behavior. The result of TEM revealed a small poly notch at the bottom of the gate electrode. This poly notch created the asymmetrical behavior and subsequent imbalance between the left and right side driver transistors. In this case, the defect was not "visible" with SEM nor SCM/SSRM analysis but easily explained by the nanoprobing data which lead to conclusive TEM cross section (see Figure 7 and 8).

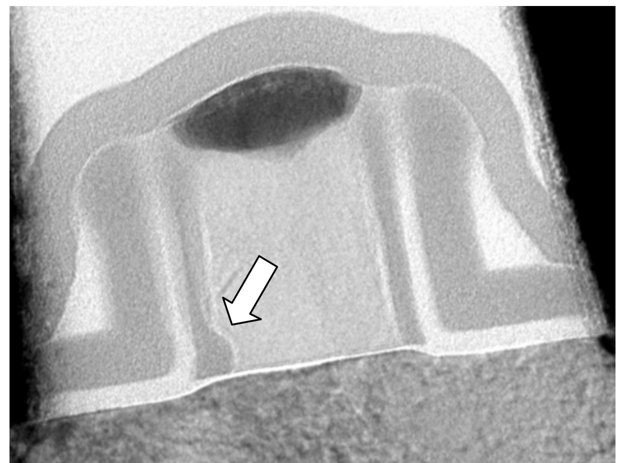

Figure 7. TEM cross section of a failing transistor shows a poly notch at the left bottom corner.

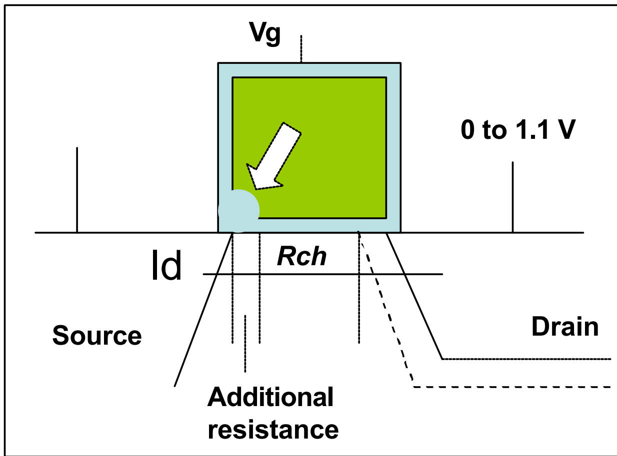

Figure 8. Probe data and TEM result correlated with observed asymmetrical behavior. The poly notch causes weak inversion or even in depletion under low gate voltages.

Sample C

In the case of sample C, several top down SEM inspections were performed on a voltage sensitive single bit failure but all results were non-visual. SCM/SSRM was performed on the failing bit and a leakage path was identified from gate to the source/drain (see Figure 9). Nanoprobing was performed at the contact level to validate the SCM/SSRM findings. The nanoprobe result confirmed that there was a resistive short from gate to source/drain of the PMOS transistor (see Figure 10). In this case, both SCM/SSRM and nanoprobing identified the same failing transistor.

This failure mechanism was attributed to a gate oxide integrity issue. Physical characterization of the ultra-thin gate oxides by top down or backside deprocessing is very challenging due to selectivity issues with current FA methods using choline based etchants.

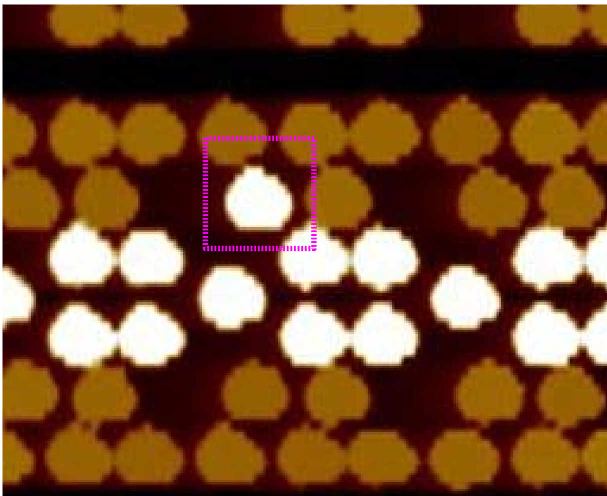

Figure 9. SCM/SSRM image shows gate contact (box) has the same leakage behavior as the source and drain of a p-channel transistor when Vtip=-1.2V.

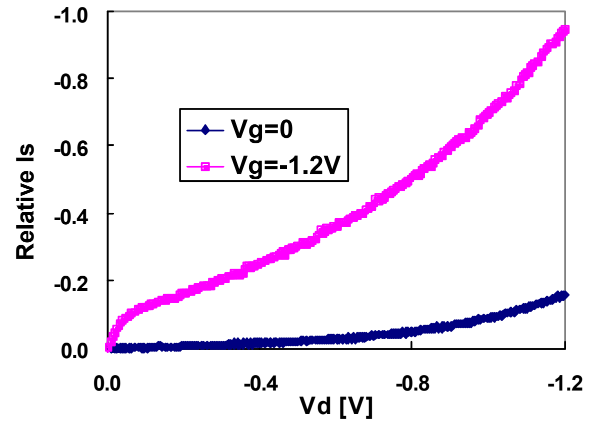

Figure 10 Is-Vd curves of failing PMOS at different Vg.

Conclusions

In this presentation, we have demonstrated the successful use of both SCM/SSRM analysis and internal nanoprobing technique for fail site isolation. We have also shown that without one or the other, the FA result might not be very conclusive. With the combination of both, we have found small silicon dislocations, gate profile defects, gate oxide integrity issues and other defects which were previously non-visual during standard PFA inspections. Our experience has suggested that these softer mechanisms and non-visual defects are becoming more and more common at sub-100nm technologies.

Acknowledgments

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References

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[2] Veeco, Inc., Santa Barbara, CA.
[3] Multiprobe, Inc., Santa Barbara, CA.
[4] Zyvex Inc., Richardson, TX.
[5] Kilby Center TEM lab, Dallas, TX.