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Atomic Force Probing in Analog MOSFETs Measurement

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Abstract

Accurately measuring parameter mismatch for analog MOSFETs, such as the threshold voltage (V_t) or *W/L* ratio, is often required in analog circuit failure analysis. The challenge in probing analog MOSFETs using atomic force probing (AFP) is contact resistance. Contact resistance between AFP tips and tungsten contacts can cause large error at high current. This paper discusses measurement error caused by contact resistance and the techniques to identify and reduce the contact resistance effect.

Introduction

High volume production of system on chip (SOC) designs on advanced CMOS technology nodes requires the ability to solve not just memory and logic problems but analog problems as well. The combination of analog circuit functionality with advanced CMOS process geometries has required improvements to the toolsets and methodologies used to solve analog circuit problems. Analog circuit problem solving must occur at both the circuit and the transistor levels in order to be effective. Even in advanced CMOS, node voltage probing at the circuit level can be done using focused ion beam (FIB) pads. But for transistor level measurement, using FIB to modify individual transistors can cause parametric shifts in V_t by ion beam charging [1]. Fundamentally, FIB pads are not a solution for transistor-level probing on advanced CMOS SOC designs. Nano-probing techniques are becoming a routine failure analysis tool for technologies from 130 nm to 65 nm. Existing nano-probing tools include atomic force probing (AFP) and SEM based nano-probing.

The use of AFP on 90-nm and 65-nm technology nodes has been reported by several authors [2-3]. However, the previous work has focused on digital MOSFETs in SRAM cells. In probing SRAM cells, the challenges are to place tips on tungsten contacts that are very close to each other and to reduce drift. In principle, if a tool can successfully probe SRAM, it should be able to probe any transistors in the same technology node.

On the other hand, analog MOSFETs usually have gate length and width equal to or greater than 1 μm. There are often more than one source/drain contacts. Spacing between the source, drain and gate contacts are greater than that in SRAM cells. This makes it easier to probe analog transistors than to probe SRAM cells from a geometrical point of view.

However, probing analog transistors has a different challenge due to the electrical precision required. It is common that the failure of analog circuits is due to parametric mismatch between pairs of transistors. The mismatch of interest may be as small as a few mV in threshold voltage (V_t) or a few percent of *W/L* ratio. Thus, V_t measurement should be accurate to 1 mV in order to distinguish a few mV V_t mismatch between two transistors. Contact resistance affects accuracy of the measurements for current higher than 10 μA. This paper will discuss the influence of contact resistance on parameter measurements and how to use the AFP to obtain reliable parameters for analog MOSFETs with accuracy sufficient for solving analog circuit problems on SOC devices..

Contact resistance effect on V_t measurement

AFP Tip Contact Resistance

The AFP system used in this work is a 4-head AFP system from Multiprobe. There are 2 types of tips, 100-nm tip for 65 - 90 nm technologies and 250-nm tip for 130 nm technology. A new AFP tip often has a contact resistance ranging from 30 to 100 Ω [4]. Contact resistance changes during scanning and probing. It can increase to more than 150 Ω after use.

The resistance of a tungsten AFP tip with a profile shown in Fig. 1 can be calculated using

$$R = \rho \int_0^L \frac{dl}{\pi r^2} \quad (1)$$

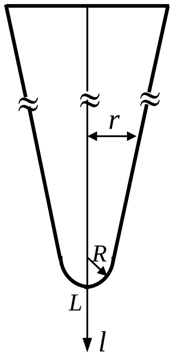

Figure 1: AFP tip profile used to estimate tip resistance.

where r is the radius of the tip at the distance l, ρ=5.5x10^{-6} Ωcm is the resistivity of tungsten and L is the total length of the tip. A typical tungsten AFP tip has a resistance of a few Ohms depending on contact area, the size and the shape of the tip. Any contact resistance above 10 Ω is extrinsic and may be caused by a barrier layer between a tip and tungsten contact. Therefore, sample surface and tip cleanness is critical to obtain low contact resistance.

Contact Resistance Effect in Saturation V_t Measurement

The influence of contact resistance on measurements depends on the magnitude of the current. Usually gate and backgate contact resistance can be ignored because of low gate and backgate current. Source and drain contact resistance (as shown in Fig. 2) cannot be ignored when source and drain current is high. If source or drain contact resistance (R_C) is 100 Ohm and source/drain current is 100 μA, voltage drop on each R_C is 10 mV. The actual gate source voltage (V_G – $V_{S'}$) is debiased by 10 mV relative to the applied V_G – V_S and the actual drain voltage $V_{D'}$ is also debiased 10 mV relative to the applied V_D. When a MOS transistor is in the saturation region ($|V_{GS}–V_t| < |V_{DS}|$), I_D is not sensitive to drain voltage. Thus drain contact resistance is not important in the saturation region. Source contact resistance cannot be ignored, however. For NMOS, saturation V_t is usually obtained by fitting I_D versus V_{GS} data to the following MOSFET equation

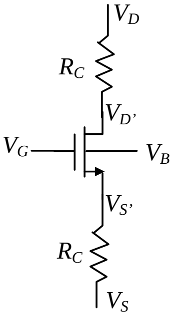

Figure 2: An NMOS with source and drain contact resistance.

$$\sqrt{I_D} = \sqrt{\frac{\mu_n C_{OX}}{2}\frac{W}{L}}(V_{GS} - V_t) = \sqrt{\beta}(V_{GS} - V_t) \qquad (2)$$

where $\beta \equiv (\mu_n C_{OX})(W/L)/2$.

With source contact resistance R_C, Eq. (2) can be modified as

$$\sqrt{I_D} = \sqrt{\beta}(V_{GS} - I_D R_C - V_t) \qquad (3)$$

Equation (3) can be rewritten as

$$\sqrt{\beta} R_C I_D + \sqrt{I_D} - \sqrt{\beta}(V_{GS} - V_t) = 0 \qquad (4)$$

Solving Eq. (3) for $I_D^{1/2}$ and using $\sqrt{1+x} \approx 1 + x/2 - x^2/8$ and $4\beta R_C(V_{GS} – V_t) << 1$ gives

$$\sqrt{I_D} = \frac{-1 + \sqrt{1 + 4\beta R_C (V_{GS} - V_t)}}{2\sqrt{\beta} R_C} \approx \sqrt{\beta}(V_{GS} - V_t) - \beta^{3/2} R_C (V_{GS} - V_t)^2 \qquad (5)$$

The first term is the original expression of Eq. (2). The second term is the error caused by contact resistance R_C.

Consider a transistor with V_t=0.5V and β =7x10^{-4} A/V^2. Fig. 3 shows square root of I_D vs. V_{GS} curves calculated according to Eq. (5) for R_C =0 Ω and R_C =100 Ω, respectively. The data range in Fig. 3 is between 0.7 V and 0.9 V. For a MOSFET with V_t = 0.5V, V_t and β are often extracted from $I_D^{1/2}$ vs. V_{GS} in this voltage range. The drain current I_D in Fig. 3 ranges from 30 – 110 μA. The curve with R_C =100 Ω gives lower β and lower V_t from curve fitting to Eq. (2).

Figure 4 shows ΔV_t=V_t – V_{t0} and $\Delta\beta/\beta_0$ extracted according to Eq. (2) from curves calculated using Eq. (5) for the transistor with different contact resistance, where V_{t0} and β_0 are reference values with R_C=0 Ω.

According to Fig. 4, in the current range of 30 – 110 μA, every 20 Ω contact resistance reduces V_t by 1.3 mV and β by 1.6%. For transistors with higher β values, the effect becomes more prominent. If drain current is in the range of 100 - 400 μA, 20 Ω contact resistance can cause 3 – 5 mV error in V_t measurement. Roughly for current ≤100 μA, to obtain less than 1.3 mV error in saturation V_t measurement and less than 1.6% error in β measurement, contact resistance variation from one transistor to another should be less than 20 Ω. The variation of contact resistance from one transistor to another is more critical than the absolute value of the contact resistance. For example, if R_C = 50 ± 10 Ω, V_t can still be measured to ~1 mV relative error if current does not exceed 100 μA, although ideal contact resistance is ~10 Ω with ±10 Ω variation.

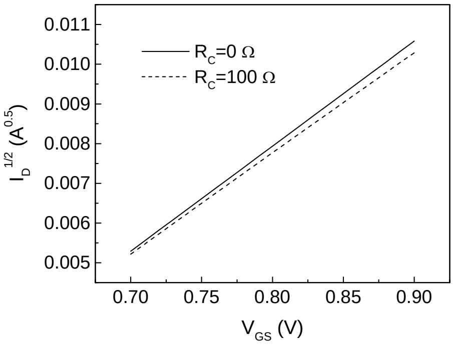

Figure 3: Square root of I_D vs. V_{GS} calculated using Eq. (4) for R_C=0 and R_C=100 Ω, respectively. Here we use typical transistor parameters V_t=0.5 V and β=7x10^{-4} A/V^2.

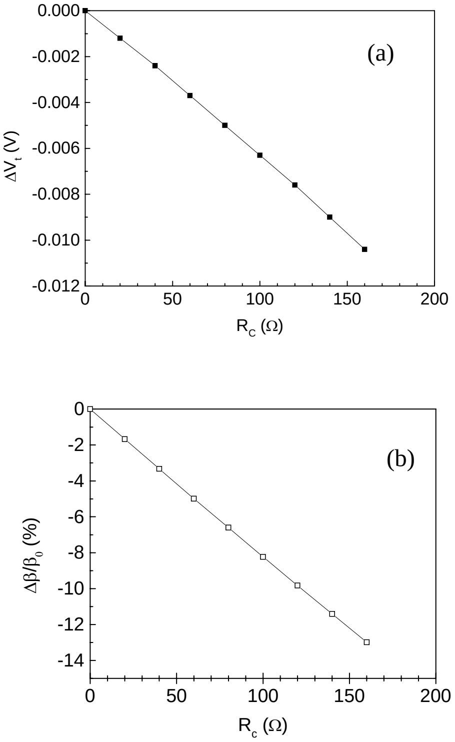

Figure 4: (a)V_t and (b)β error caused by contact resistance in saturation V_t measurement. Here we use typical transistor parameters V_t=0.5V and β =7x10^{-4} A/V^2.

Contact Resistance Effect in Linear V_t Measurement

Linear V_t measurements are performed by fitting I_D – V_{GS} curves with the MOSFET equation in the triode region ($|V_{GS} - V_t| > |V_{DS}|$)

$$I_D = \beta[2(V_{GS} - V_t)V_{DS} - V_{DS}^2] \tag{6}$$

Linear V_t is obtained by extrapolating the I_D – V_{GS} curve to I_D = 0.

$$V_t = V_{GS}\Big|_{I_D=0} - 0.5V_{DS} \tag{7}$$

Assuming that the source and drain have the same contact resistance R_C, triode region I_D - V_{GS} curve can be written as

$$I_D = \beta[2(V_{GS} - I_D R_C - V_t)(V_{DS} - 2I_D R_C) - (V_{DS} - 2I_D R_C)^2] \tag{8}$$

Solving Eq. (8) for I_D gives

$$I_D = \frac{\beta[2(V_{GS} - V_t)V_{DS} - V_{DS}^2]}{1 + \beta R_C[4(V_{GS} - V_t) - 2V_{DS}]} \tag{9}$$

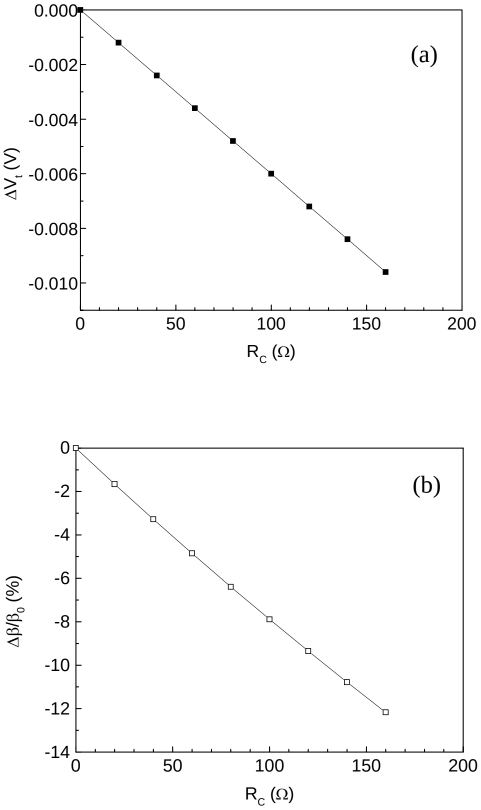

Figure 5: (a) V_t and (b) β error caused by contact resistance in linear V_t measurement. Here we use typical transistor parameters V_t=0.5V and β=7x10^{-4} A/V^2.

Similar to Eq. (5), with contact resistance the slope of the I_D – V_{GS} curve is reduced and the interception of the I_D – V_{GS} curve to I_D = 0 is also reduced. Using the same technique as in the saturation case, we can obtain ΔV_t and $\Delta\beta/\beta_0$ caused by different contact resistance in linear V_t measurement. Figure 5 shows ΔV_t and $\Delta\beta/\beta_0$ versus contact resistance for the same transistors discussed in the saturation case. The current range in which V_t and β are extracted is about 15 – 30 μA, where V_{GS} ranges 0.65 – 0.75 V. From Fig. 5, if the drain current is in the range of 15 – 30 μA, every 20 Ω contact resistance will cause a 1.2 mV error in V_t and 1.5% error in β. In linear V_t measurement, therefore, the error caused by contact resistance for the same transistor is about the same as would be caused in a saturation V_t measurement. In general, to compare linear V_t between transistors to 1 mV relative error, contact resistance variation from one transistor to another should be less than 20 Ω if drain current is between 15 and 30 μA.

V_t Measurement Using AFP

It can be estimated by using the same method in the last section that if the drain current is less than 4 μA in linear V_t measurement or less than 10 μA in saturation V_t measurement, 100 Ω contact resistance causes roughly 1 mV error in V_t and

1% error in β. It is possible to obtain less than 100 Ω contact resistance variation from one transistor to another. Therefore, when drain current is lower than 4 μA in a linear V_t measurement or lower than 10 μA in a saturation V_t measurement, contact resistance is not a big problem. However, many analog transistors are wide ($W/L >> 1$), so the current of interest in the linear and saturation regions may exceed this range.

Use Subthreshold Current as a Reference

For higher drain current, measurement error depends on the magnitude of the drain current and contact resistance variation. Contact resistance is usually unknown in measurements. How can we identify whether extracted V_t and β values are affected by contact resistance? One way is to compare the V_t difference between two transistors obtained in the linear or saturation region to mismatch in the subthreshold region ($|V_{GS}| < |V_t|$).

Fig 6(a) shows $I_D^{1/2}$ versus V_{GS} curves measured using AFP for two 130-nm node NMOS in the saturation region. From the linear portion of the $I_D^{1/2}$ - V_{GS} curves, we obtained V_t and β listed in Table 1. Since the linear portion of the curves is in the range of 40 – 110 μA, every 20 Ω contact resistance will cause ~1mV V_t error. To determine whether V_t and β mismatch between the two MOSFETs are correct, we can use subthreshold current plot as shown in Fig 6(b). Subthreshold currents in Fig. 6(b) are below 1 μA, so a contact resistance of even as high as a few hundred Ohms can be ignored. Therefore, subthreshold current usually has no contact resistance effect and can be used to justify the correctness of the measurements.

In the subthreshold region, the difference between the two I_D – V_{GS} curves reflects true mismatch between the two transistors. From Fig. 6(b), V_{GS} of NMOS2 is about 10 mV less than V_{GS} of NMOS1 for a given current, indicating V_t of NMOS2 is about 10 mV less than V_t of NMOS1. This is close to 8.3 mV V_t difference shown in Table 1. In this example, error caused by contact resistance is small. The majority of the extracted ΔV_t therefore reflects the actual parametric mismatch of the MOSFETs.

If V_t and β from the high current portion of I_D – V_{GS} data do not correlate with the subthreshold current plot, then contact resistance may have a high variation from one transistor to another in the measurements. V_t and β obtained from the high current portion of the curve thus do not reflect the actual parametric mismatch between transistors. In this case, subthreshold current plots can be used to find transistor mismatch.

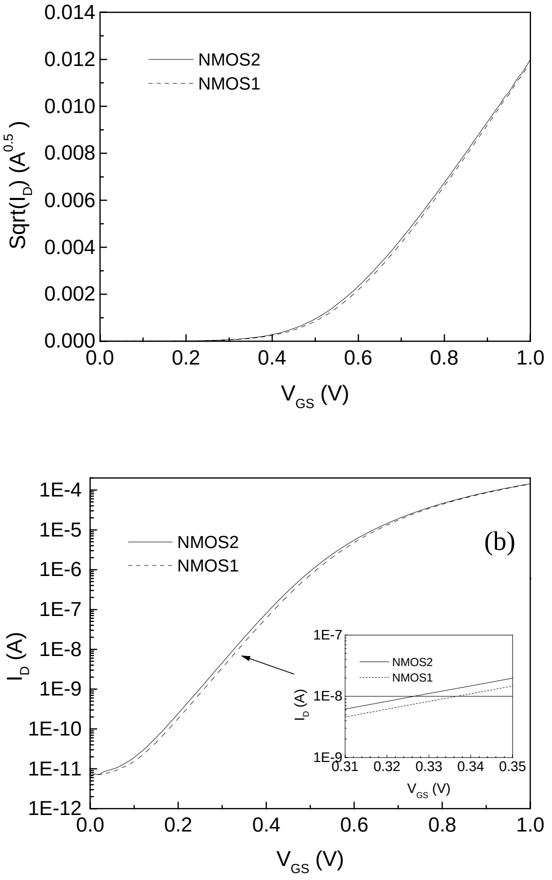

Figure 6: (a) Square root of I_D versus V_{GS} and (b) subthreshold current plots for two 130-nm NMOS measured using AFP.

Table 1: V_t and β values obtained from saturation V_t measurement using AFP on two 130-nm NMOS.

	V_t (V)	ΔV_t (V)	β (A/V^{-2})	$\Delta\beta/\beta$ (%)
NMOS1	0.5499		6.92x10^{-4}	
NMOS2	0.5416	-0.0083	6.78x10^{-4}	-2.01

In the traditional subthreshold method, V_t is determined by the voltage at which the curve of logI_D – V_{GS} plot departs from linearity [5]. For mismatch measurements, however, it is difficult to determine the departure point with ~1mV accuracy on logI_D – V_{GS} curves. Since we are looking for mismatch, absolute values of V_t are not critical. The difference of logI_D – V_{GS} plots between two MOSFETs such as Fig. 6(b) provides mismatch information. However, in subthreshold current plots, it is not easy to separate V_t and β contributions, which can be seen as follows. For $V_{DS} \geq 0.1$V, subthreshold current, I_{Dst}, can be written as [6]

$$I_{Dst} = \frac{\mu_n (kT)^2 W}{q^2 L} C_D \exp[\frac{q(V_{GS} - V_t)}{\xi kT}]$$

(10)

where $\xi = (1 + C_D/C_{OX})$ and C_D is depletion region capacitance. Taking the log of Eq. (10) gives

$$\log I_{Dst} = \log[\mu_n (kT/q)^2 C_D] + \log(W/L) + \frac{q(V_{GS}-V_t)}{\xi kT}\log e \quad (11)$$

If subthreshold current plots for two transistors are parallel as in Fig. 6(b), then ξ is the same for the two transistors. If we assume a typical value of ξ=1.3, then for 1mV V_t mismatch, logI_{Dst} will shift by 0.013. We also can cause the same shift in logI_{Dst} by assuming a 3% *W/L* mismatch. In other words, a 3% *W/L* mismatch is equivalent to a 1 mV V_t mismatch in its impact on subthreshold current. Therefore, for a small mismatch in V_t or *W/L*, it is not easy to distinguish the respective contributions of V_t and *W/L* using only subthreshold plots. For large mismatch of one parameter, however, it is not difficult to determine the dominant contribution. For instance, if there is a 10 mV or higher mismatch for a given current in the subthreshold region as in Fig. 6(b) and there is no large β mismatch apparent in the high current portion of the $I_D - V_{GS}$ curve, then one can conclude that most of the 10 mV must come from V_t mismatch. For *W/L* to cause a 10 mV mismatch in subthreshold current, *W/L* mismatch should be around 30%, which is easy to be observed at high current region.

Use Sensing Probe

The best way to eliminate the contact resistance effect is to put second tip on the source and drain to sense source and drain voltages. This is possible on analog MOSFETs because analog MOSFETs often have more than one contact on source and drain. However, sensing source and drain voltage requires additional probes. For saturation V_t measurement, drain contact resistance is not important if the slope of $I_D - V_{DS}$ is small, so sensing source voltage is enough in most cases. For NMOS that is not isolated from the substrate, we can free the backgate probe and use it to sense source voltage because backgate grounding can be realized by grounding the Si substrate. For PMOS, however, n-well contact is necessary. Therefore, a fifth probe is needed to sense source voltage. It requires putting 5 AFP heads in the AFP system.

Use 250-nm Tip

In probing an SRAM cell, typical AFP tip size is ~100nm, which allows tip placement on tungsten contacts with only ~100nm spacing. Since analog transistors have enough space, we can use 250-nm tips to probe MOSFETs of both 130-nm and 90-nm nodes. As illustrated in Fig. 7, a 250-nm tip becomes flat after scanning and probing. The image of contacts becomes large when the tip becomes flat. As long as individual contacts can be distinguished, however, low image quality does not matter. The advantages of 250-nm tips are longer lifetime, more stable contact, and the fact that a 250-nm tip will not bend during use. It only becomes flat, providing a large area for contact, thereby reducing the effect of drift. In principle, the tip resistance of 250-nm tips is lower than that of 100-nm tips according to calculation using Eq. (1). However, in reality, contact resistance of 250-nm tip is not found to be better than that of 100-nm tip. This is probably because contact resistance is dominated by an extrinsic barrier layer between the tip and tungsten contacts. If the barrier layer can be overcome, we may get lower contact resistance from a 250-nm tip than for a smaller tip.

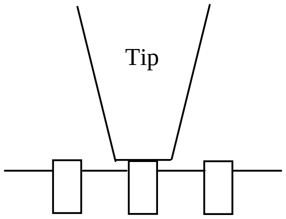

Figure 6: Illustration of 250-nm tip making contact on tungsten contacts

Conclusions

Contact resistance in atomic force probing affects accuracy of V_t and β measurements for analog MOSFETs. Contact resistance variation from one transistor measurement to another causes error in finding parameter mismatch between MOSFETs. The influence of contact resistance depends on the magnitude of the current. For saturation V_t measurement, every 20 Ω contact resistance reduces V_t by 1.3 mV and β by 1.6% if the drain current is in the range of 30 – 110 μA. In linear V_t measurement, contact resistance causes the same amount of error as in saturation V_t measurement.

Subthreshold current plots can be used to identify whether V_t and β mismatch obtained from the high current portion of $I_D - V_{GS}$ curves is altered by contact resistance. A subthreshold current plot itself can be used to find transistor mismatch in many cases. The best way to eliminate contact resistance effects is to use an additional probe to sense the source voltage in saturation V_t measurement. Finally, 250-nm tip provides longer lifetime and better stability in probing analog MOSFETs.

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