Scanning Capacitance Microscopy at transistor contact level.

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Introduction

Traditionally planar scanning capacitance microscopy has been conducted on samples which have been deprocessed to the level of the substrate and an oxide re-grown over the sample. A drawback of the technique lies in the fact that HF used to etch the sample to the substrate can also dissolve shallow junctions. In this contribution we document the ability of scanning capacitance microscopy to be utilized at the level of the contacts leaving the pre metal dielectric intact. By deprocessing to this level shallow junctions will still be left intact. We demonstrate the scalability of this technique across three process generations spanning 0.18 micron, 0.13 micron and 90 nm nodes. Preliminary data on anomalous contrast observed in contacts at both 0.13 micron node and 90 nm node products is documented. The ability to distinguish between contacts going to a n type diffusion, p type diffusion and transistor gate is demonstrated. Some precautions to be observed when the sample is prepared for this analysis are also highlighted. The final section of the paper discusses a simple conceptual model for the CV curve of a defective contact connected to the depletion capacitance of a source /drain diffusion of a transistor.

Section 1 Evolution of contact level SCM imaging

As mentioned in the introduction above traditionally SCM has been used to image diffusions in either the planar or cross sectional mode by deprocessing to the level of the substrate accompanied by oxide re- growth. As technology progressed from the 0.25 micron through the 0.13 micron generation the depths of the junctions were reduced and the dopant concentration increased. In our experience HF (hydrofluoric acid) that was used to etch the sample from the poly silicon level to the level of the substrate was contributing to junction loss at the 0.25 micron node and little or no signal could be obtained using this method of sample preparation at the 0.18 micron node. We also experimented with deprocessing the sample to the level of the gate oxide with a choline based etch but with this route the etch was difficult to end point, and the resulting images difficult to interpret due to sample preparation artifacts. The problem was also compounded with concerns about the safety of choline use in a laboratory environment. A third alternative we pursued with some success was to obtain wafer samples from the fab that had been processed only to the level of the gate oxide and image these samples with SCM. This route proved successful in isolating implant related issues[1]. However in practice since the majority of the samples that arrived at our laboratory were full loop samples returned from the customer or reliability fallout, the above mentioned method was not an all encompassing solution. During the 0.18 micron node product ramp it became increasingly clear that we would need a method to look at via and contact related issues. This lead to an experiment in which a sample was polished to be deliberately non planar and SCM imaging performed on this non planar sample. We could obtain SCM signal from both the contacts and poly- silicon portion of the sample, (see Fig 1). The contact level images however suffered from image quality problems (mainly related to streaks in the image) . As will be mentioned later in this paper the image quality dramatically improved when we switched from Iridium coated tips to Tungsten wire type tips.

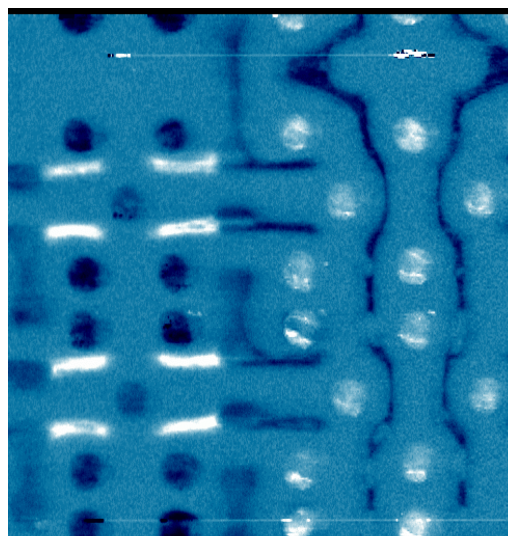

Fig 1. Scanning capacitance image of a 0.18 micron technology node sample deprocessed to the level of polysilicon. The contacts going to n type diffusions are in white, those going to p type are in brown. The polysilicon fingers can also be delineated.

Section 2 Scalability to the 0.13 and 90 nm nodes

The method of deprocessing samples to the level of the contacts was found to scale across process generations. In particular it was found that we could image contacts at both the 0.13 micron generation of products and the 90 nm generation of products. Fig 2 and 3 show contact level SCM imaging of a 0.13 micron node and a 90 nm node product respectively. Both the images have been taken with a Tungsten wire type tip. The Iridium coated tips did not produce images with good spatial resolution at the 0.13 micron node and their use was not attempted at the 90 nm process node.

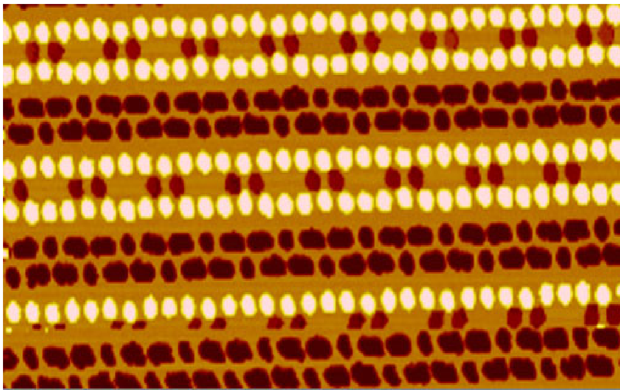

Fig 2 Contacts in the memory regions of a 0.13 micron node product imaged with scanning capacitance.

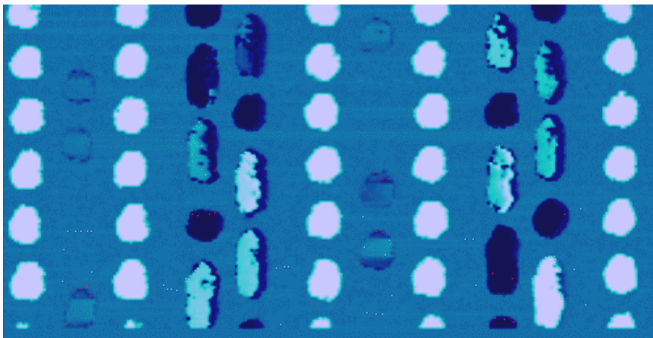

Fig 3 Contacts in the memory regions of a 90 nm node product imaged with scanning capacitance.

The tungsten wire tips were found to be essential for the 0.13 and 90 nm node imaging, as they produced images of contacts with startling contrast. The one disadvantage experienced with Tungsten wire tips was their tendency to damage the sample when poly- silicon level imaging was attempted. The Iridium coated tips were capable of producing poly silicon level images at the 0.18 micron node, but had insufficient spatial resolution for finer geometries. However repeated experiments even at very low deflection set point(0.05 volt) at the poly silicon level on both 0.13 micron and 90 nm products with Tungsten wire cantilevers resulted in sample damage. Fig 4 shows an SEM image of the Tungsten wire probes used for imaging.

Sample prep for contact level SCM integrates well into the normal deprocess flow. The process flow adopted for the preparation of the samples was to etch the ILD levels with a RIE and manually polish the metal levels. When the sample was destined for the SCM though no FIB marking was performed below metal 3 and all SEM imaging prior to the contact level was performed at or below 1 Kv. It is generally advantageous to have natural land marks to navigate to the site of interest but in dense memory arrays laser marking or FIB marking of the failing bit is inevitably required. In such cases we have found the guide lines mentioned above to be necessary for generating usable samples.

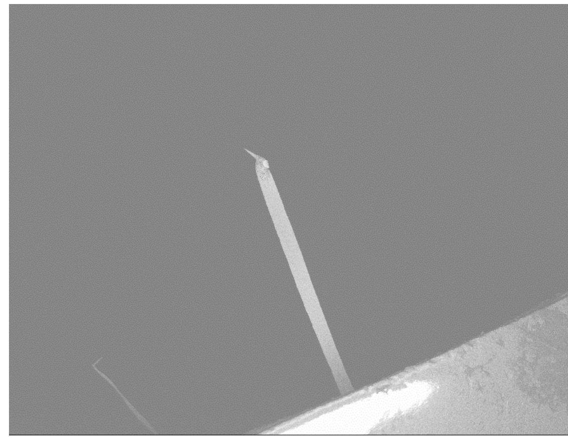

Fig 4 SEM image of Tungsten wire tip used for SCM on 0.13 micron and 90 nm node silicon.

Section 3 Contacts going to N, P type diffusions and transistor gates show distinct contrast.

Examination of the Fig 3 shows contacts with three distinct colors. On examination of the layout database we ascertained that these contacts are connected to distinct diffusion types and transistor gates respectively. The contacts appearing white go to N type source/drain diffusions, while the ones appearing maroon go to P type source /drain diffusions. The reason for variation of the contrast observed on the P type diffusion in the picture is not entirely clear. Two plausible explanations have been forth coming in the course of internal discussions. One of them related to systematic dopant concentration fluctuations in the P type source/drain diffusions. The second has to do with the SCM acquisition electronics. It is speculated that stretch P contacts of the nature shown in Fig 3 resistively loads the resonant circuit used to sense the capacitance and causes the resonance characteristic of the circuit to be altered leading to the variations observed. The intermediate (yellow/ brown) contacts go to transistor gates. A simple model for the capacitance sensed in the case of a source /drain type diffusion contact and a MOSFET gate contact will be presented in the final section of the paper. It is perhaps the differing nature of the capacitance sensed in each case that causes the contacts to appear in distinct colors.

Section 4 Examples of anomalous SCM contrast observed in contact level samples.

In this section of the paper we will present three examples of anomalous contrast observed in samples de-processed to the contact level. All three examples have to do with memory failures. The first example is a part at the 0.13 micron process node that failed several columns of the memory. The second and third examples are single bit memory failures. In one case the part was at the 90 nm node and physical de-processing revealed a defect at the transistor level. In the final case the part was a 0.13 micron node product in which a short between a transistor gate contact and a N well tap contact is suspected.

Figures 5(a) and (b) illustrates the SCM contrast observed from a contact in a failing column write driver and one from a good column write driver. The part was a 0.13 micron node device and failed several columns in a memory array. A transistor gate contact in the case of the failing column write driver showed anomalous contrast as opposed to a similar contact in a good column driver. The scan size is smaller in Fig 5(b) as compared to Fig 5(a) by a factor of 2 and emphasizes the distinct anomalous contact in the case of the bad column write driver. Both images were obtained with a DC bias of 0.6 volt. It was confirmed by circuit tracing that the anomalous gate contact could explain the observed electrical failure signature. TEM cross- sectioning of the anomalous contact was attempted but unsuccessful due to loss of the relevant sample area. However the utility of SCM in such cases is evident as voltage contrast in a SEM is of limited use when contacts to transistor gates are involved.

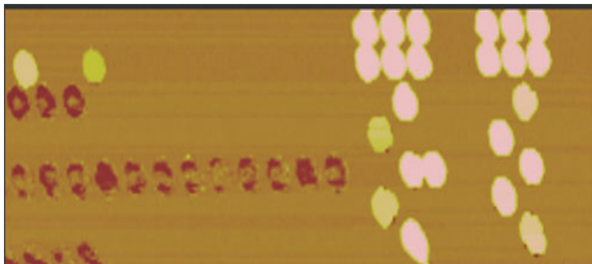

Fig (a) SCM imaging of contacts from a good write driver.

Fig 5 (b) SCM imaging of identical contacts from a bad write driver. The arrow shows the location of the bad contact.

The second example is a 90 nm node product that failed a single bit of memory in a cache array. The sample was de-processed to the contact level through a combination of RIE etching to remove the ILD and mechanical polishing to remove the metal. Since natural landmarks were available for counting to the affected bit, no FIB marking was necessary. When the contact level was reached no SEM examination was performed. SCM imaging immediately revealed anomalous contrast from several contacts in the isolated bit area. Given the size of the area displaying anomalous contrast, it was decided that planar de-processing to poly-silicon would be the best route to pursue. Prior to further de-processing voltage contrast was attempted in a SEM without success, indicating once again the ability of SCM to pick up defects not necessarily isolated by SEM voltage contrast. On de-processing to the level of poly silicon a gate moat short was discovered at the location of one of the contacts showing anomalous contrast. Figures 6(a) and (b) show the SCM image of the anomalous contacts and an SEM picture of the defect that caused the single bit failure.

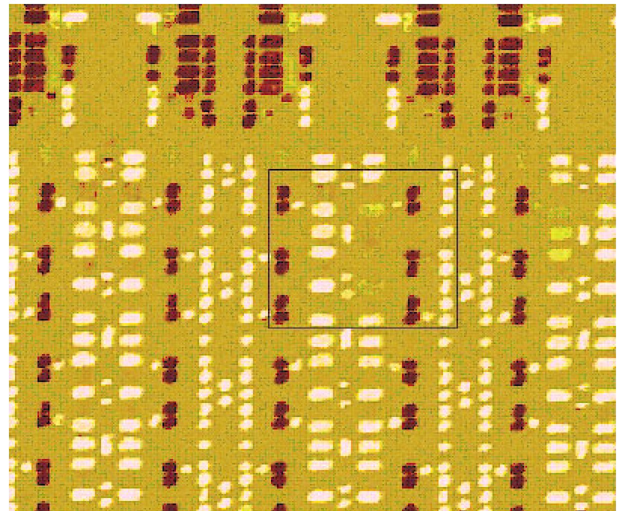

Fig 6(a) SCM image showing contacts with anomalous contrast on a 90 nm product exhibiting a single bit failure.

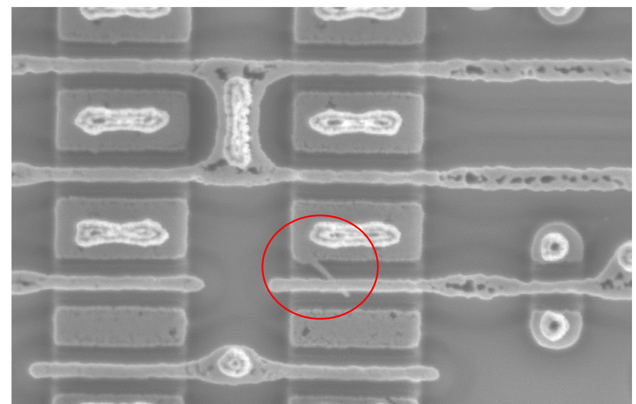

Fig 6(b) SEM image showing gate moat short that caused the single bit failure. The defect lies within the box in Fig 6(a) that shows anomalous contrast.

The final example is of a single bit failure, this time in a 0.13 micron node microprocessor part that failed a single bit of memory in a cache array. SCM showed anomalous contrast at a gate contact. Since the gate contact showed the same contrast as a N well tap right below it, it was surmised that the anomalous contrast could be due to one of two reasons. The first reason could be an intrinsic problem with the gate contact itself. The second alternative explanation could be a short between the gate contact and the N well tap. A FIB section through the defective contact did not show any anomalies. TEM investigation of similar samples however did show the presence of dislocations and their presence is thought to be responsible for the single bit failure. Fig 7 shows the SCM image with the anomalous region circled. The upper contact is the gate contact and the lower contact is a N well tap contact. The image was obtained at 0.6V DC bias.

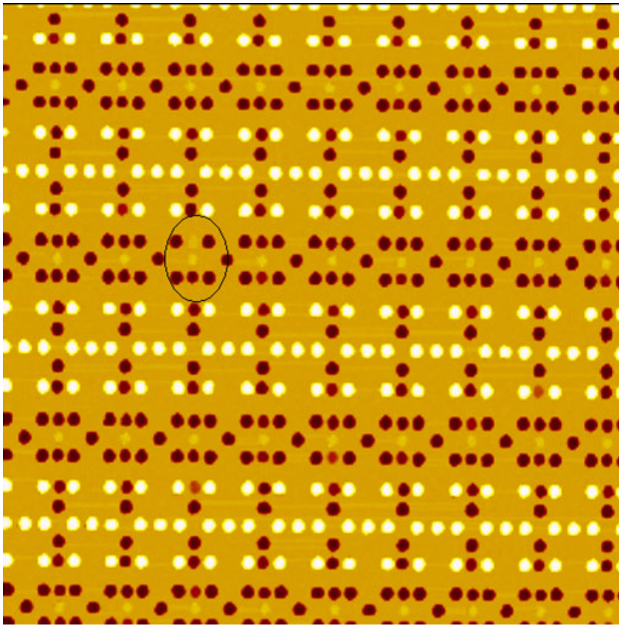

Fig 7 Anomalous contrast observed at the gate of an invertor(circled) in a cache array of 0.13 micron node micro processor. The upper contact is a gate contact and the lower contact is a N well contact.

Section 5 Stacked Via 1 imaging with SCM.

In the special case of stacked via1 it is possible to obtain SCM images at via 1. This possibility is illustrated in Fig 8 where a 0.13 micron node device has been de-processed to the level of via 1 through a combination of RIE etching and polishing of metal levels. In essence the previous two sections have pointed to the ability of SCM to be useful at both the contact level and possibly at the via 1 level.

Section 6 Simple electrical models for SCM imaging of transistor source/ drain contacts and gate contacts.

We have seen earlier that the contacts gong to a P or N type source/drain diffusions appear in different contrast as compared to the contacts that go to the gate of a transistor. In this section we provide a simple electrical model to rationalize this difference. This section is conceptually divided into two parts. In the first we examine the different capacitance contributions in the case of a contact going to the gate of a transistor as opposed to that in the case of a contact going to the source/drain diffusion of a transistor. In the second part we explore with a very simple model the effect on the CV curve of a defect in a contact going to a N type source/drain diffusion.

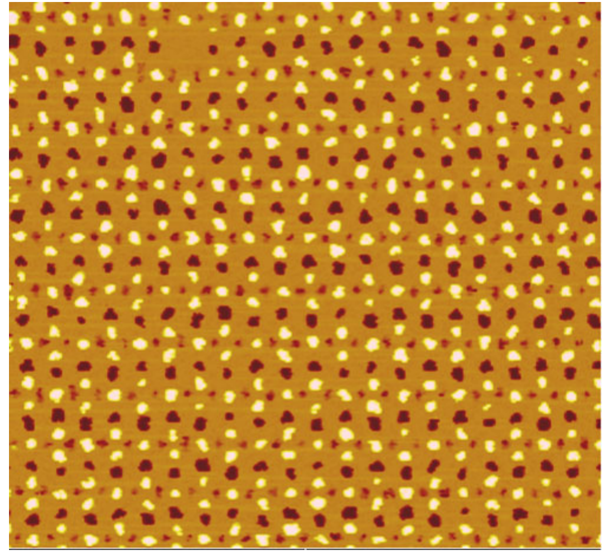

Fig 8 SCM imaging at the via 1 level in a memory array of a 0.13 micron node device.

In the case of a contact going to the source/drain diffusion of a transistor the contact serves as an extension of the probe tip coupling to the depletion capacitance of the PN junction formed by the source/drain diffusion and the well/substrate. As the DC bias is changed different portions of the CV curve of the depletion capacitor are sampled. In the case of a contact going to the gate of a transistor, the contact serves as an extension of the probe tip that probes the MOS capacitor formed by the gate dielectric and the underlying channel with the contact as the gate electrode. In the case of a well diffusion we have an additional PN junction related depletion capacitance in series with MOS capacitor. Since the CV characteristic of above mentioned cases are different (PN junction depletion capacitance in one case as opposed to a MOS capacitor in series with a depletion capacitor in the other) different contrast is expected from a contact going to a gate as opposed to one going to a source/drain diffusion.

It is possible to computationally explore the effect of introducing a defect in the contact going to a N type source/drain diffusion of a transistor with the help of a very simple model illustrated in Fig 9(a). The introduction of a

defect in the contact adds an air gap capacitor is series with the depletion capacitance of the PN junction[2]. The size of the air gap can be varied and the capacitance voltage curve can be computed for the series combination. Since it is the gradient of the CV curve that is sensed in SCM we can rationalize the reason for the observation of anomalous contrast from defective contacts. Fig 9 (b) exhibits the CV curves when defects of varying sizes are introduced. It is clear from the graph that when a small air gap (< 1 nm) is introduced most of the voltage of the source is dropped across the depletion capacitor of the PN junction and the CV curve is characteristic of the depletion capacitor. On the contrary when we introduce a larger air gap (~ 1 micron) into the contact, most of the voltage now drops across the air gap defect capacitor. Since the defect capacitance has a value independent of voltage we see a flat CV curve. Since it is DC/DV that is imaged in scanning capacitance this latter case should not give any signal. This simple model helps us explain the utility of SCM in isolating defective contacts.

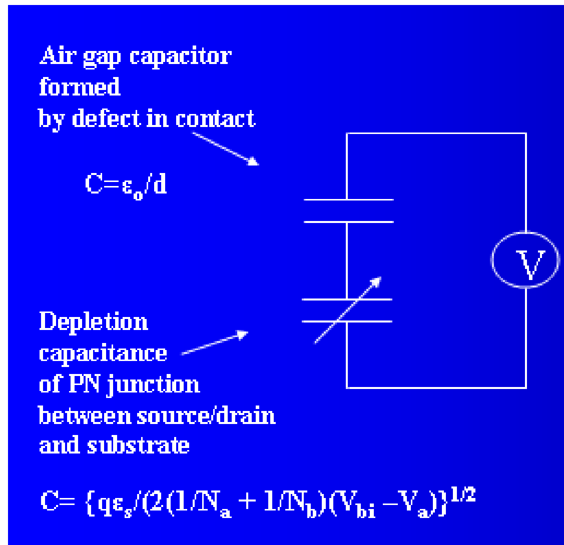

Fig 9 (a) Simple conceptual model for a defective contact connecting to the depletion capacitance of a source/drain diffusion.

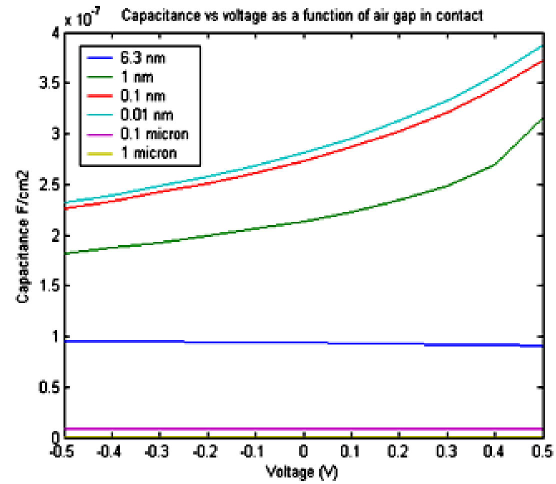

Fig 9 (b) CV voltage curves as a function of the air gap in the defective contact. Note the flat curve for micron sized gaps.

Summary and Conclusions

In summary and conclusion we have demonstrated the ability to get useful information about contacts with Scanning capacitance microscopy. The scalability of the technique to 90 nm geometries and the ability to work at via 1 have been demonstrated. A simple model for the CV curves of defective contacts to source/drain diffusions has been presented.

Acknowledgements

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References

1. Ramanujachar.K. submission to EDFAS Photo contest 2001.
2. Muller.R., Kamins.I. Theodore;‘ Device Electronics for Integrated Circuits’ Second Edition. John Wiley