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SCANNING ELECTRON MICROSCOPE INDUCED ELECTRICAL BREAKDOWN OF TUNGSTEN WINDOWS IN INTEGRATED CIRCUIT PROCESSING

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Abstract

Interaction of inline SEM inspections with tungsten window-1 integrity were investigated. Multiple SEMs were utilized and various points in the processing were inspected. It was found that in certain circumstances inline SEM inspection induced increased window-1 contact resistance in both source/drain and gate contacts, up to and including electrical opens for the source/drain contacts.

1. Introduction

As device dimensions steadily decrease in integrated circuit manufacturing, the use of scanning electron microscopy (SEM) has increasingly replaced optical microscopy for defect detection and defect analysis. Yet, the interaction between the electron beam, the surface scanned, and the further processing of the die is relatively unknown. A recent incident, however, challenged the assumption that in-line SEM inspection is electrically innocuous. The defects in Figure 1 were reviewed with a SEM after window-1 tungsten CMP. After a post-inspection wet clean, it was observed that a line of tungsten windows to N-source/drain that were previously intact were now cored. It appeared that the SEM had triggered corrosion of the plugs along the path the SEM took traveling from one defect to the next (Figure 2).

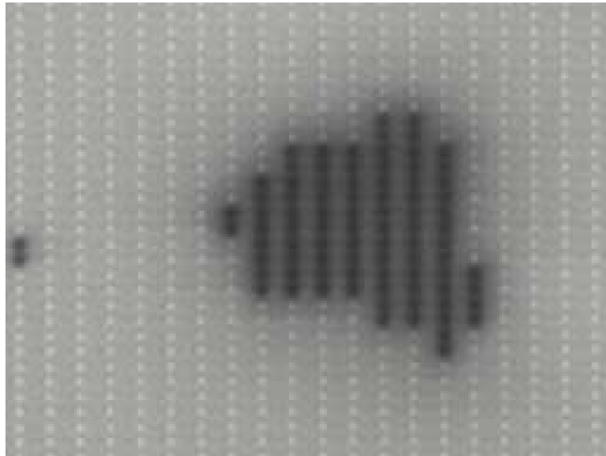


Figure 1: SEM Inspection of Processing Defect At Window-1 Level, After Tungsten CMP

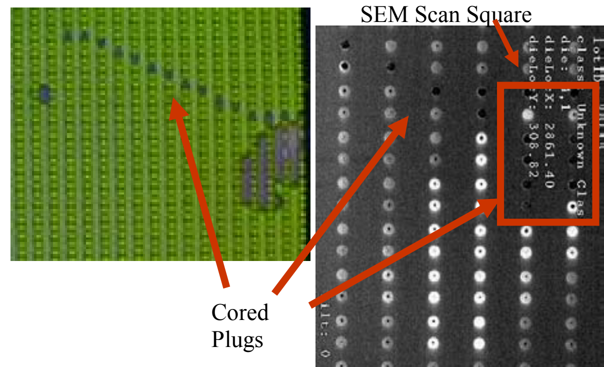


Figure 2: Same Defect as Figure 1, after Post-SEM Clean - The Tungsten Plugs Are Cored Where the SEM Beam Impinged (Optical and SEM Images.)

A study was undertaken to determine what, if any, implications SEM imaging of an in-process wafer has on the electrical integrity of the scanned areas. Attention was focused on the tungsten window-1 module.

Section 2 describes the experimental methodology including the SEMs used and the processing steps at which the wafers underwent inspection. Section 3 describes the results including the IV data and physical analysis. The conclusions are discussed in Section 4 including a brief consideration of physical failure mechanisms, and future directions of study.

2. Experimental

The SEMs
The SEMs used in this study are currently in common use in modern IC fabs. The first SEM is a model ES20XP scanning E-beam inspection system manufactured by KLA-Tencor. The beam conditions used for this SEM were acceleration voltage of 800eV, and a probe current of 66 nanoamperes. The second SEM is a SEMVision CX manufactured by Applied Materials, using an acceleration voltage of 1000eV, and a probe current of 58 picoamperes. The third SEM is a model JWS 7515 wafer inspection system manufactured by JEOL, using an acceleration voltage of 2500eV and probe current of 10pA. The field of view for the ES20 was 10µm by 10µm, for a total scanned area of 100µm2. The field of view

for the SEMVISION was 3µm by 3µm, for a total scanned area of 9µm2. The field of view for the JEOL was 3.25µm by 2.5µm for a total scanned area of 8.125µm2. For the SEMVISION and JEOL, the dwell time on each site was 17 ± 1 second. For the ES20, the dwell time on each site was 328 milliseconds. Multiplying the probe current by the scan time and dividing by the scan area yields the total electron dose per square micron. As such, the calculated doses are for the ES20 1.35E+09 electrons/µm2, for the SEMVISION 6.84E+8 electrons/µm2, and for the JEOL 1.31E+8 electrons/µm2. These details are summarized in Table 1.

Table 1: SEM Scanning Conditions for the Five Stitches in Experiment One

SEM	Vacc	Probe Current	Field of View	Scan Area	Scan Time	Total Electron Dose electrons/µm^2
ES20XP	800eV	66nA	10µm X 10µm	100 µm^2	328 msec	~1.35E+09
SEMVision CX	1000eV	58pA	3µm X 3µm	9 µm^2	17 sec	~6.84E+08
Jeol JWS7515	2500eV	10pA	3.25µm X 2.5µm	8.125 µm^2	17 sec	~1.31E+08

The Test Structures

Two wafers (wafers 01 and 02) were processed through metal-1, capped and pulled from the line for electrical testing and analysis. The wafer layout consists of a total of 76 flash fields laid out in 10 rows by 11 columns. Figure 33 depicts the wafer with row labels. Row 1 and 10 did not undergo SEM inspection at any time. Rows 2 and 3 underwent ES20 inspection. Rows 4 and 5 underwent JEOL inspection. Rows 6 and 7 underwent SEMVISION inspection. Rows 8 and 9 underwent inspection by all three SEMs at precisely the same spots on the stitches so that the inspections overlapped.

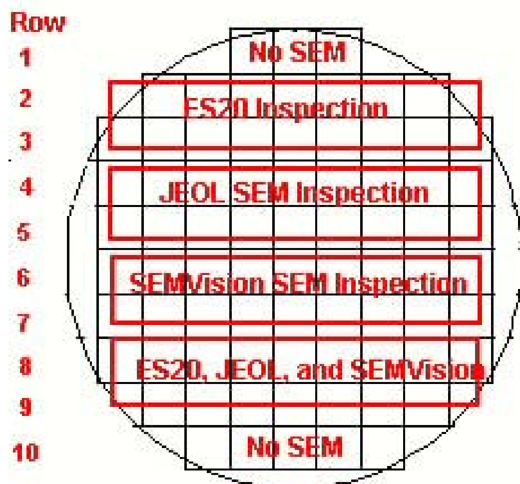


Figure 3: Wafer Layout Identifying SEM Inspection Row

The two silicon wafers were processed to dielectric one. SEM imaging was performed on a total of five different window-1 stitches. A stitch is a two-point test structure with 2000 windows at nominal sizing, connected in series such that any single open contact will cause the entire structure to fail. There was a 2000 window stitch for each of the following types of windows:

- Wn-1 between Mtl-1 and 1.5V N+-Source/Drain in P-Tub
- Wn-1 between Mtl-1 and 1.5V P+-Source/Drain in N-Tub
- Wn-1 between Mtl-1 and 3.3V N+-Source/Drain in P-Tub
- Wn-1 between Mtl-1 and 3.3V P+-Source/Drain in N-Tub
- Wn-1 between Mtl-1 and 1.5V N-doped gate stack.

The layout of the source/drain stitch is seen in Figure 4. There are 2000 windows laid out at 0.20µm X 0.20µm. The metal pads are 0.24µm in width with a 0.02µm extension on either side of the window and an extension beyond window of 0.06µm.

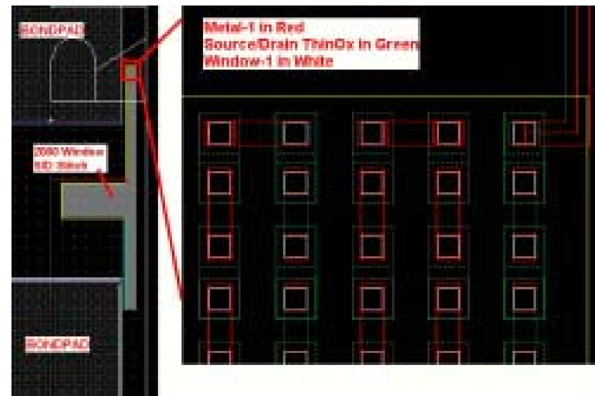


Figure 4: Schematic of 2000-Window Source/Drain Stitch

The Processes Inspected

The battery of SEM scans were performed at four points in the processing. These scan points were:

- Scan Area 1: On the oxide of dielectric-1, after Wn-1 pattern and plasma etch and clean, prior to Wn-1 IMP Ti/TiN liner deposit
- Scan Area 2: After Wn-1 IMP Ti/TiN liner deposition prior to CVD tungsten deposition
- Scan Area 3: After Wn-1 tungsten CMP and clean prior to Metal-1 stack deposition
- Scan Area 4: After metal-1 patterning and etch

The four areas of the stitches scanned by the SEMs are indicated in Figure 5. It should be noted here that metal-1 was intentionally misaligned in both the X and Y direction by ~80µm. This amount of misalign is the upper limit of the specification for overlay tolerance and will allow for the underlying plug to be exposed. This can be seen in the final SEM image of Figure 5. To restate, this amount of overlay is within the technology specification. After the two wafers completed the fourth run of SEM inspections, they were split.

One wafer received a post-metal wet clean, and then dielectric caps were deposited. The second wafer did not receive the wet clean, but went directly to caps deposition after SEM scan #4. Either process fell within the normal process flow of this technology.

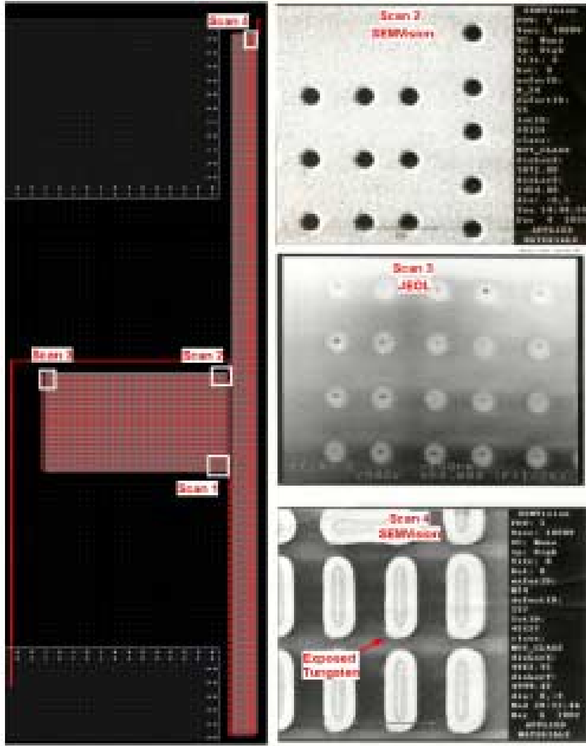


Figure 5: SEM Scan Locations after (1) Window Etch, (2) Window Liner Deposition, (3) Tungsten CMP, (4) Metal-1 Etch, With Accompanying SEM Image

After caps were deposited on metal-1 and caps were patterned, the two wafers were pulled from the line along with additional wafers from the same wafer lot to be used as controls. All wafers then underwent IV testing.

2. Results and Discussion

IV Results

The electrical resistance of the 2000 window-1 stitches for each of the five window-1 types is presented in the following five figures and five tables

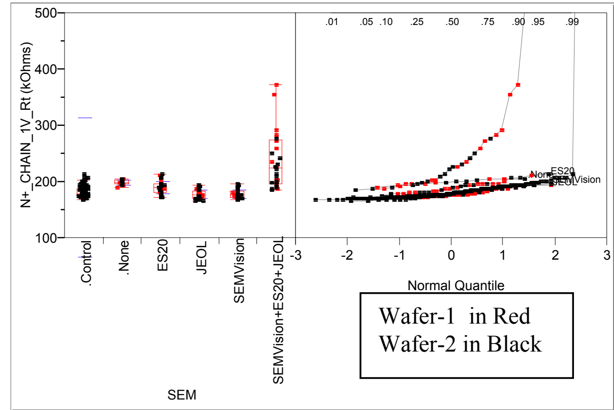


Figure 6: Oneway Analysis of Win-1 to 1.5V NSD Stitch Resistance By SEM Inspection, With Quartile Plot

Table 2: Total Resistance Mean, Standard Deviation, and Quartiles of The Win-1 to 1.5V NSD Stitch Resistance By SEM Inspection (Units of Kilohms)

					Quantiles					
Level	Number	Mean	Std Dev	Min	10%	25%	Median	75%	90%	Max
.Control	218	190.0	123.5	168.7	171.8	174.7	179.5	187.8	194.7	2000.0
.None	12	199.5	4.6	191.3	192.2	195.7	199.2	204.2	205.5	205.7
ES20	32	189.8	11.0	172.5	175.5	181.0	189.5	196.4	208.2	213.3
JEOL	36	178.2	7.9	166.8	168.6	170.6	177.2	184.1	190.9	194.5
SEMVision	36	178.1	7.9	168.6	169.2	172.3	176.4	183.4	191.3	197.0
SEMVision+ES20+JEOL	30	15734.5	84841.4	185.9	187.8	196.2	225.1	274.5	370.6	464940.0

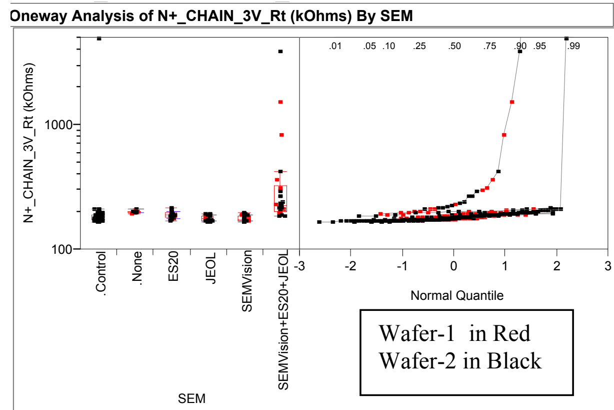


Figure 7: Oneway Analysis of Win-1 to 3.3V NSD Stitch Resistance by SEM Inspection, With Quartile Plot

Table 3: Total Resistance Mean, Standard Deviation, and Quartiles of the Win-1 to 3.3V NSD Stitch Resistance By SEM Inspection (Units of Kilohms)

					Quantiles					
Level	Number	Mean	Std Dev	Min	10%	25%	Median	75%	90%	Max
.Control	218	9.18E+07	1.35E+09	168.1	171.0	174.1	179.6	188.5	196.6	2.00E+10
.None	12	201.9	4.9	195.9	196.0	198.0	201.0	204.6	211.1	213.6
ES20	32	189.6	11.7	171.3	174.2	180.3	189.0	196.9	207.5	216.8
JEOL	36	178.0	8.4	166.5	167.9	170.4	176.4	185.3	191.0	195.2
SEMVision	36	178.1	8.9	167.4	168.4	171.8	175.4	184.1	193.9	199.5
SEMVision+ES20+JEOL	30	1.67E+05	6.48E+05	186.2	188.68	202.28	228.4	326.3	363.5	3.00E+06

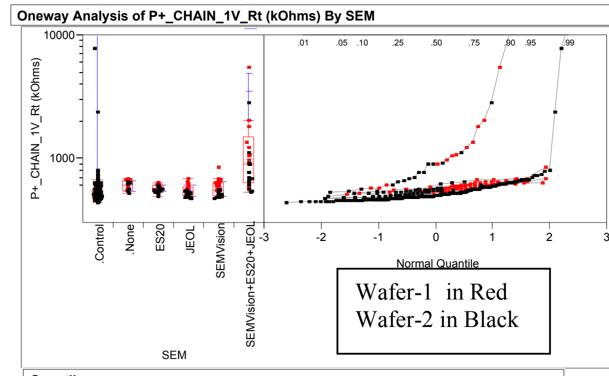


Figure 8: Oneway Analysis of Win-1 to 1.5V PSD Stitch Resistance By SEM Inspection, With Quartile Plot

Table 4: Total Resistance Mean, Standard Deviation, and Quartiles of the Win-1 to 1.5V PSD Stitch Resistance By SEM Inspection (Units of Kilohms)

					Quantiles					
Level	Number	Mean	Std Dev	Min	10%	25%	Median	75%	90%	Max
.Control	218	1.38E+06	2.03E+07	437.5	459.8	476.3	500.8	562.7	634.0	3.00E+08
.None	12	606	57.8	520.6	526.1	556.7	607.9	664.2	683.1	686.8
ES20	32	571	39.8	493.8	520.8	533.6	571.4	607.8	628.1	641.0
JEOL	36	546	54.3	475.2	480.0	500.7	537.9	589.7	622.6	683.3
SEMVision	36	572	80.0	478.2	487.9	500.6	555.0	630.2	663.6	856.0
SEMVision+ES20+JEOL	30	3442	7808.2	536.4	565.4	641.1	901.4	1484.5	9572.1	34254

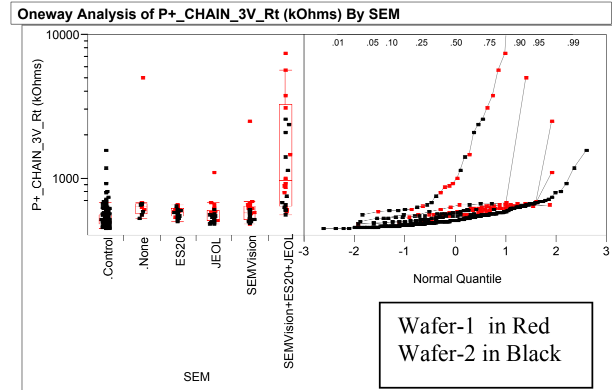


Figure 9: Oneway Analysis of Win-1 to 3.3V PSD Stitch Resistance By SEM Inspection, With Quartile Plot

Table 5: Total Resistance Mean, Standard Deviation, and Quartiles of The Win-1 to 3.3V PSD Stitch Resistance By SEM Inspection (Units of Kilohms)

					Quantiles					
Level	Number	Mean	Std Dev	Min	10%	25%	Median	75%	90%	Max
.Control	219	539	108	449.1	466.7	484.2	509.4	561.2	636.0	1572
.None	12	980	1260	532.2	538.3	562.1	642.3	661.2	3689	4979
ES20	32	582	40	501.5	531.7	545.6	582.0	614.7	638.0	653.7
JEOL	36	568	103	479.5	493.4	508.6	551.2	593.9	649.0	1090
SEMVision	36	630	326	483.8	496.7	515.5	575.2	640.7	663.7	2498
SEMVision+ES20+JEOL	30	271795	1141549	560.2	601.0	643.4	961.9	3276	70857	6000000

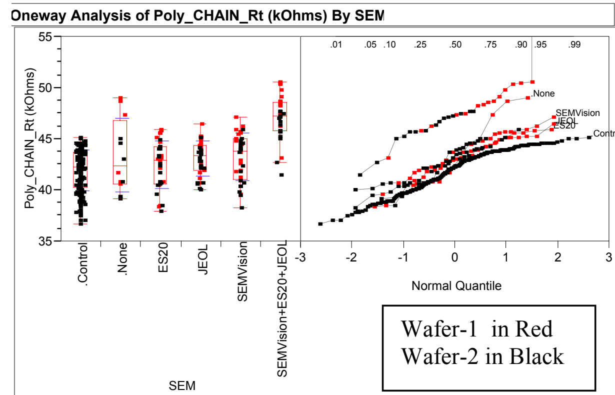


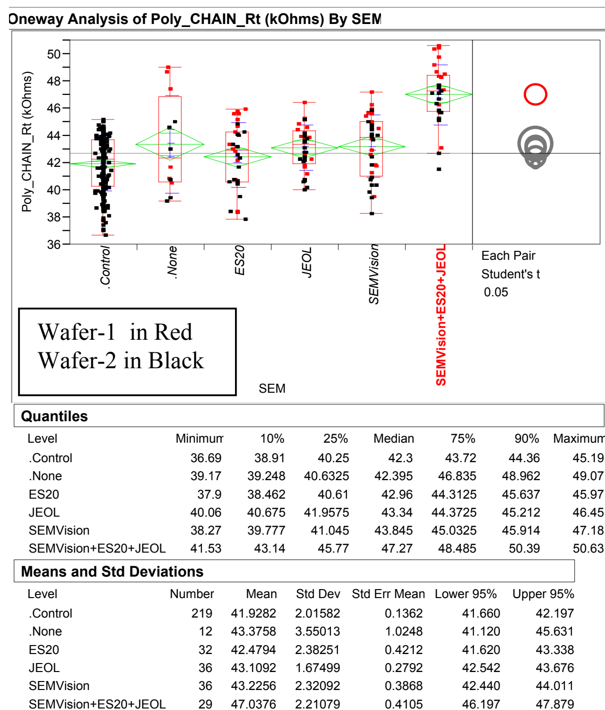
Figure 10: Oneway Analysis of Win-1 to Poly-Silicon Gate Stack Stitch Resistance By SEM Inspection, With Quartile Plot

Table 6: Total Resistance Mean, Standard Deviation, and Quartiles of The Win-1 Poly-Silicon Gate Stack Stitch Resistance By SEM Inspection (Units of Kilohms)

					Quantiles					
Level	Number	Mean	Std Dev	Min	10%	25%	Median	75%	90%	Max
.Control	219	41.93	2.02	36.69	38.91	40.25	42.30	43.72	44.36	45.19
.None	12	43.38	3.55	39.17	39.25	40.63	42.40	46.84	48.96	49.07
ES20	32	42.48	2.38	37.90	38.46	40.61	42.96	44.31	45.64	45.97
JEOL	36	43.11	1.67	40.06	40.68	41.96	43.34	44.37	45.21	46.45
SEMVision	36	43.23	2.32	38.27	39.78	41.05	43.85	45.03	45.91	47.18
SEMVision+ES20+JEOL	30	1245	6561.5	41.53	43.34	45.80	47.33	48.61	50.44	35986

It is evident from quartile plots for the four thinox stitches, that the sites that received SEM inspection by all three SEMs have considerable disturbances in resistance. The mean, median and standard deviation of the stitch resistance for the combined cell is significantly greater than any of the other cells of the experiment as well as the control cell. While the upper and lower quartiles for all but the combined SEM NSD stitches fall between approximately 170 and 200 kΩ for both the 1.5V and 3.3V, the NSD quartiles for the combined SEM cell fall between ~200 and 325kΩ. While the upper and lower quartiles for all but the combined SEM PSD stitches fall between approximately 475 and 650 kΩ for both the 1.5V and 3.3V, the PSD quartiles for the combined SEM cell fall between ~640 and 3300 kΩ. In addition, for the four source/drain stitches approximately 10% of the combined SEM structures have measured resistances in the megohms up to and including electrical opens. For the other five cells the few opens that occurred were obvious outliers and the distributions were much tighter. Scanning electron microscope imaging has caused the electrical failure of window-1 to source/drain contacts.

For the window-1 stitch to gate, there is also a statistically significant increase in measured resistance, however, the gate stitches did not show the high number of catastrophic failures that the source/drain stitches showed. Figure 11 replots the window-1 to poly stitch excluding a single outlier data point from the combined SEM cell.



Quantiles

Level	Minimum	10%	25%	Median	75%	90%	Maximum
.Control	36.69	38.91	40.25	42.3	43.72	44.36	45.19
.None	39.17	39.248	40.6325	42.395	46.835	48.962	49.07
ES20	37.9	38.462	40.61	42.96	44.3125	45.637	45.97
JEOL	40.06	40.675	41.9575	43.34	44.3725	45.212	46.45
SEMVision	38.27	39.777	41.045	43.845	45.0325	45.914	47.18
SEMVision+ES20+JEOL	41.53	43.14	45.77	47.27	48.485	50.39	50.63

Means and Std Deviations

Level	Number	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%
.Control	219	41.9282	2.01582	0.1362	41.660	42.197
.None	12	43.3758	3.55013	1.0248	41.120	45.631
ES20	32	42.4794	2.38251	0.4212	41.620	43.338
JEOL	36	43.1092	1.67499	0.2792	42.542	43.676
SEMVision	36	43.2256	2.32092	0.3868	42.440	44.011
SEMVision+ES20+JEOL	29	47.0376	2.21079	0.4105	46.197	47.879

Figure 11: Oneway Analysis of Win-1 to Poly-Silicon Gate Stack Stitch Resistance By SEM Inspection, Excluding a Single Outlier Point From Combined SEM Cell

In this case, the mean of the combined SEM cell increased from ~43kΩ to ~47kΩ as compared to the other experimental cells, which is an increase of only ~9%. In addition, the standard deviation remained similar between the cells with no increased spread in the distribution of the resistances for the combined SEM cell. This percentage increase may seem inconsequential, but if it can be assumed that only one of the four scan points was responsible for the increase (not necessarily a safe assumption) then that 4kΩ resistance was caused by a scan area of only a few square microns, encompassing twenty windows or less. This is, potentially, an average increase of 200Ω per contact, for a gate contact resistance that normally measures ~10 Ω per contact.

In summary, inline SEM inspection of window-1 test structures by multiple SEM inspections on the same tester caused significant increases in contact resistance, up to and including electrical opens. This phenomenon occurred on five different types of window-1 test structures on two separate wafers.

Physical Analysis

PVC imaging was attempted in order to isolate some of the failing windows. This method has been used with great success in locating failing windows between metal levels as well as windows to gate. Unfortunately, no voltage contrast imaging was detectable from the source/drain stitches. It is speculated that the charge build up that should occur on the floating side of the stitch is dissipated by the junction leakage of the N+ to Ptub or P+ to Ntub junctions underneath the window-1 contacts.

Multiple random FIB cross-sections were then taken from failing stitches. The locations of the cuts were the four scan areas as detailed in
Figure 5. A representative STEM for each of the four scan areas on a failing PSD stitch can be seen in
Figure 12.

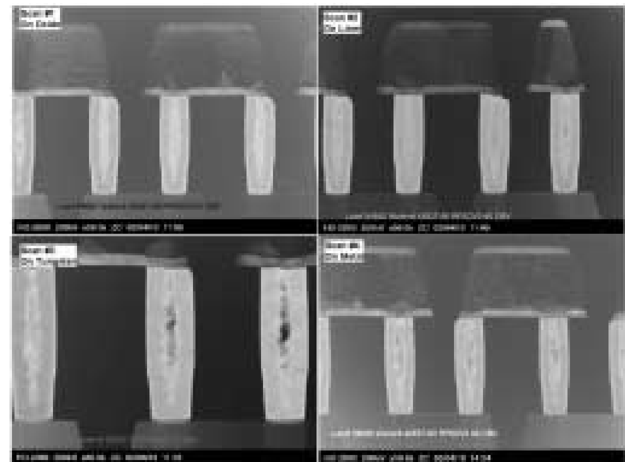


Figure 12: Scanning TEM Cross-Sectional Micrographs of the Four SEM Scan Areas From Electrically Open Failing Stitches

The random cross-sections did not identify either the failure locations or the failure mechanism. In fact, cross-sections indicate well formed and filled windows, with no apparent foreign interfaces, between silicon and liner, between liner and tungsten, or between tungsten and Ti/TiN barrier.

Multiple failing stitches were then deprocessed by CHF_3 plasma etch of the caps. The metal-1 aluminum was then etched away in an HCl bath, and the Ti/TiN barrier was polished off via CMP. Top-down SEM images of these failed stitches were taken.

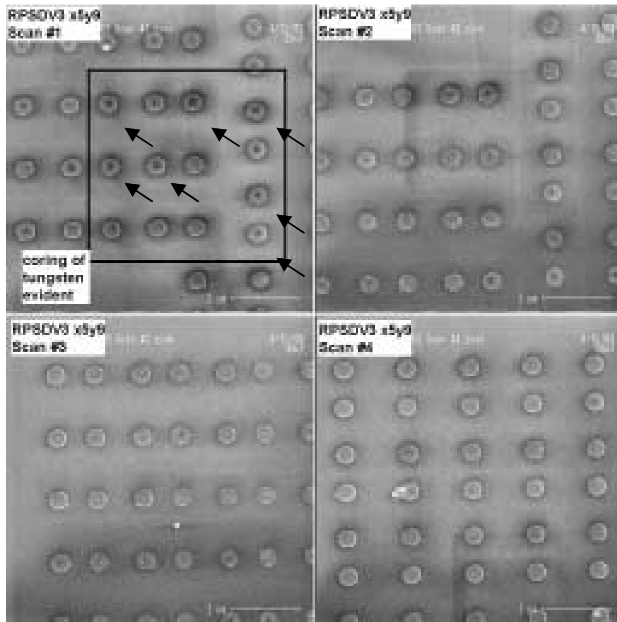


Figure 13: Top-Down SEM of the Four Scanned Areas on a Failing 3.3V PSD Stitch After the Removal of Metal-1 – Tungsten Coring Evident In Scan Area #1

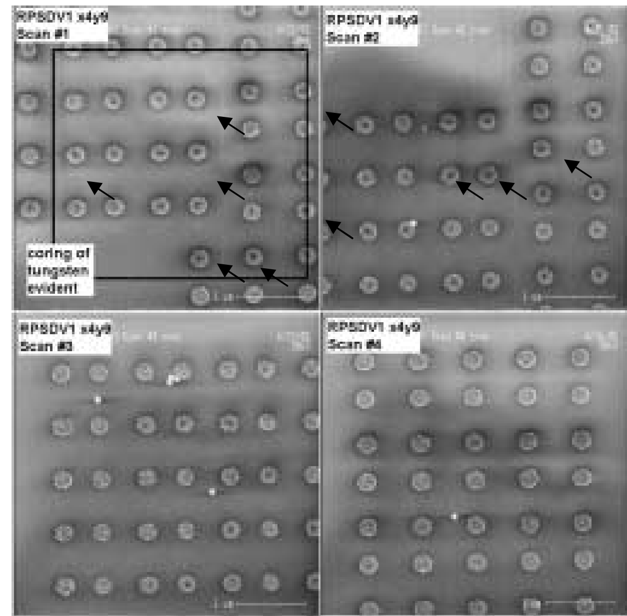


Figure14: Top-Down SEM of the Four Scanned Areas On a Failing 1.5V PSD Stitch After the Removal of Metal-1 – Tungsten Coring Evident In Scan Area #1

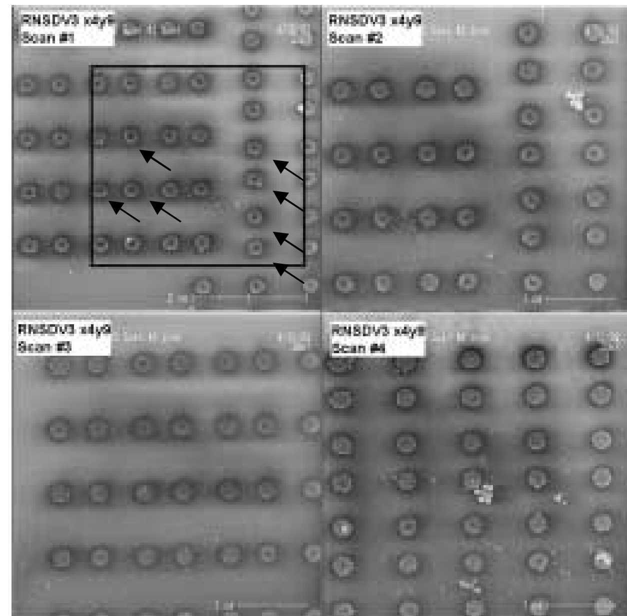


Figure 15: Top-Down SEM of the Four Scanned Areas On a Failing 3.3V NSD Stitch After the Removal of Metal-1 – Tungsten Coring Evident In Scan Area #1

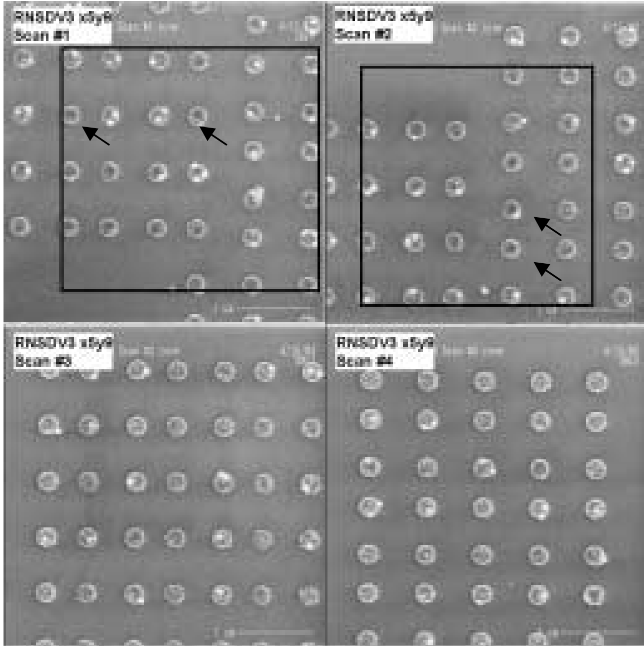


Figure 16: Top-Down SEM of the Four Scanned Areas On a Failing 3.3V NSD Stitch After the Removal of Metal-1 – Tungsten Coring Evident In Scan Area #1

Top-down SEM imaging of the failing source/drain stitches gives an indication that the source of the electrical variation may be in SEM scanning of the oxide surface (scan #1) prior to the window Ti/TiN liner. High magnification images of these windows clearly indicate incomplete tungsten fill.

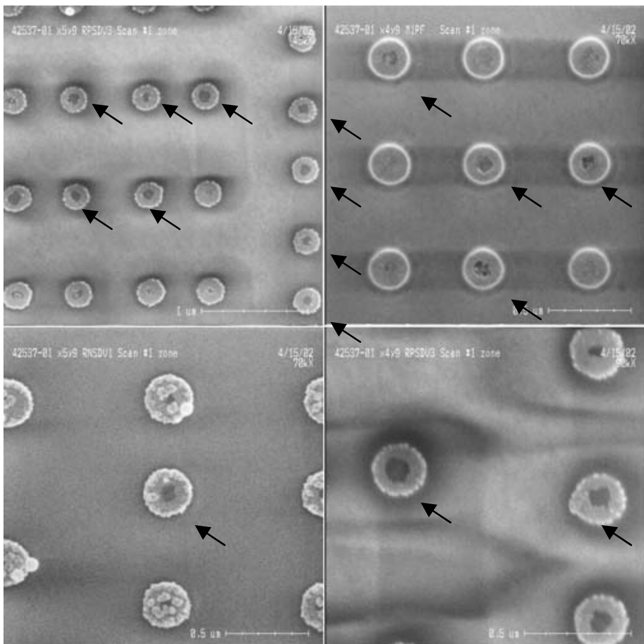


Figure 17: High Magnification SEM Images of Incompletely Filled Window-1 in Scan Area #1.

In some instances, the area that received SEM scans after liner deposition (scan #2) also showed some degree of incomplete fill. Scan areas #3 and #4 did not show any coring; rather the windows appeared to be correctly filled. Because the precise location of the failing window was not pinpointed, the incompletely filled windows must be considered circumstantial, but they are at the very least an indication of the process step which is most detrimental to submit to inline SEM inspection

4. Conclusions and Future Work

The impact of SEM inspection on IC processing integrity was investigated. An example of SEM induced electrical failure of a window-1 contact was reported. It was found that in the event of multiple SEM inspections of a source/ drain contact at various points in the wafer processing, the electrical resistance of the inspected structures increased dramatically - up to and including electrical opens.

The physical failure mechanism will most likely fall into one of three categories:

1. The SEM deposits a thin hydrocarbon interfacial film that disrupts the electrical integrity of the thin films
2. SEM interaction disrupts the normal deposition of the thin film or the normal structural integrity of the thin film
3. The SEM injects a stored charge on the sample surface that upon subsequent processing drives electrochemical/galvanic corrosion of one of the metal thin films.

The fact that source/drain stitches showed catastrophic fails and a wide distribution of resistance whereas the poly stitches showed neither catastrophic fails nor a wide distribution in resistances would argue against the first premise. A purely physical deposition of a carbon 'burn' mark would not preferentially choose a patterned oxide over thinox versus a patterned oxide over gate stack. In fact because the aspect ratio of the gate contact is less than for the S/D contact it might be expected that carbon deposition would be more detrimental to the gate contact. Likewise a hydrocarbon interface between Ti/TiN liner and tungsten or between tungsten and metal barrier, would not be expected to preferentially deposit over a thinox stitch as compared to a poly stitch.

As to the second premise, thin film perturbations, several mechanisms are conceivable that could account for the observations. Source/ drain contact resistance relies on the silicidation of the deposited Ti/TiN window liner to form an ohmic contact. For the window to gate contact, the tungsten plug is landing on a deposited metal silicide in the gate stack. Therefore Ti-silicidation is not a requirement for good ohmic contact. A hydrocarbon interface between silicon and liner could retard or prevent the silicidation reaction of the source/drain contact. This mechanism would not explain the evident coring of the plugs in the Scan #1 and Scan #2 areas, since the tungsten nucleation and deposition would not be disturbed. However, since the tungsten coring is

circumstantial the aforementioned mechanism can not be eliminated. Alternatively, a charge field injected into the oxide by the SEM prior to Ti/TiN liner deposition could impact the coherence of that liner. The impinging titanium is ionized, and therefore would be subject to electrical fields associated with the surface. The sidewall thickness of the window is on the order of only tens of angstroms, so even minor alterations of the liner deposition could lead to discontinuous coverage over the sidewall. An incoherent liner could impact the nucleation of tungsten, which would explain the cored plugs. Additionally, hydrocarbon deposition on the surface of the liner could also disrupt the nucleation of tungsten, which could explain the cored tungsten. The disruption of tungsten nucleation, would not however, be expected to occur preferentially over thinox as compared to poly, furthermore the tungsten deposition in this process is generally considered to be self-nucleating.

Finally, the third premise appears quite feasible. Stored charge driven electrochemical corrosion has been reported for both the tungsten plugs and the titanium metal barrier. In fact the observations made by Lee et al [10] agree with the electrical findings of this study: plugs electrically connected to the source/ drains failed whereas plugs terminating at gate did not. The argument against this premise is that the findings of this paper generally found completely voided windows, whereas the deprocessed stitches in this study showed only slight perturbations if any at all. Even so, the third premise seems most likely in light of the Lee finding.

Ample opportunity exists for future directions of investigation, First and probably foremost, independent corroboration of the phenomenon would be invaluable. While the conditions used in this study were entirely within the process guidelines, the SEM dwell times were particularly long: margin studies for dwell time, and beam conditions would therefore be interesting. Beyond that, investigation using a single window kelvin cross-bridge structure would be valuable in that any fails would be isolated to a single window for simple STEM analysis. The question also arises as to why only stitches from the combined cell failed. Obviously, the total electron dose is greatest for that cell, but there could also be a beam interaction involved. Namely, the Jeol SEM is operating at 2500eV which is above the crossover point, where the total number of incident electrons equals the total number of ejected electrons. For non-grounded dielectrics, electrons will be injected into the surface and the surface will develop a negative potential. On the other hand, the other two SEMs were operating below the crossover point, where more electrons are emitted than are incident, and a net positive potential will develop on the surface non-grounded dielectrics [2].

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